Cyprus University of Technology

杭州電子科技大學 HANGZHOU DIANZI UNIVERSITY

Master's thesis

Development and Validation of Compact Models for Si IGBTs and SiC MOSFETs in Power Electronic Systems

Yifan Li

Limassol, December 2025

MSc in Electronics Science and Technology

CYPRUS UNIVERSITY OF TECHNOLOGY

Faculty of Engineering and Technology

Department of Electrical Engineering, Computer Engineering, and Informatics

Master's thesis

Development and Validation of Compact Models for Si IGBTs and SiC MOSFETs in Power Electronic Systems

Yifan Li

Supervisor

Neo Lophitis

Limassol, December 2025

Approval Form

Master's thesis

Development and Validation of Compact Models for Si IGBTs and SiC MOSFETs in Power Electronic Systems

Presented by

Yifan Li

Supervisor: Neo Lophitis

Member of the committee: Committee member 1

Member of the committee: Committee member 2

Cyprus University of Technology
Limassol, December 2025

Copyrights

The approval of the dissertation by the Department of Electrical Engineering, Computer Engineering, and Informaticsdoes not necessarily imply the approval by the Department of the views of the writer.

Acknowledgements

I would like to express my sincere gratitude to all my fellow students who accompanied me to Cyprus. Their unwavering support and assistance in both academic pursuits and daily life have been invaluable throughout this journey. The camaraderie and mutual encouragement we shared made the challenges of studying abroad more manageable.

My deepest appreciation goes to my supervisor, Dr. Neo Lophitis, for his exceptional guidance and mentorship. His kindness, patience, and profound knowledge have been instrumental in shaping my research skills. Under his thoughtful direction, I have learned not only the technical aspects of research but also the mindset and approach needed for scientific inquiry. His encouragement during difficult periods and constructive feedback have been crucial to the completion of this thesis.

I am also particularly grateful to my fellow research group members for their academic support and collaborative spirit. Our numerous discussions and exchange of ideas have significantly contributed to my understanding of the subject matter. The intellectual stimulation provided by these interactions has enhanced the quality of this research and fostered my growth as a researcher.

ABSTRACT

This research addresses the challenges of accurately modeling power semiconductor devices, particularly the non-linear characteristics of IGBTs in the low-voltage region. A novel correction method based on transfer characteristics was developed and applied to both MOSFETs and IGBTs, revealing significant differences in their responses because of fundamental structural variations. The study found that while the correction method produced minimal improvements in MOSFET models (1. 83%), it dramatically improved the accuracy of the IGBT model in the low-voltage region: 12. 6% in MATLAB simulations and 21.7% in circuit simulators, with improvements up to 77.9% under specific gate voltage conditions. The research also compared NLM and Simple Derivative Implementation (SDI) capacitance modeling methods, demonstrating the superior numerical stability of NLM for complex device structures. These findings were validated through static characteristic fitting and double pulse testing. By bridging physics-oriented and mathematics-oriented modeling approaches, this research enhances the understanding of carrier transport mechanisms and conductivity modulation in different device structures, contributing to more accurate simulation tools for power electronics design. The improved models enable better prediction of device behavior in critical operating conditions, supporting advancements in applications from renewable energy to electric vehicles.

Keywords: Power semiconductor devices, IGBT modeling, transfer characteristics correction, junction capacitance modeling, wide-bandgap semiconductors

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

BJT	Bipolar Junction Transistor
DPT	Double Pulse Test
EMI	Electromagnetic Interference
GaN	Gallium Nitride
IGBT	Insulated Gate Bipolar Transistor
LUT	Look-Up Table
MATLAB	Matrix Laboratory
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NLM	Nonlinear Mapping
SDI	Simple Derivative Implementation
SiC	Silicon Carbide
SPICE	Simulation Program with Integrated Circuit Emphasis
TCAD	Technology Computer-Aided Design

1 Introduction

1.1 Aims and Objectives

The primary aim of this research is to create accurate and portable wide-bandgap semiconductor SPICE behavioral models. Power semiconductor devices, particularly MOSFETs and IGBTs, are fundamental components in modern power electronic systems, requiring precise modeling for system design and simulation. Despite significant progress in semiconductor device modeling, existing models still face challenges, especially in accurately representing the nonlinear characteristics in the low-voltage region of IGBTs.

The specific objectives of this research are:

1. To develop an improved modeling method that enhances the fitting accuracy of IGBT static characteristics in the low-voltage region while maintaining model simplicity and physical reasonableness.
2. To investigate and compare the structural differences between MOSFETs and IGBTs that lead to different responses to modeling corrections.
3. To evaluate different junction capacitance modeling methods (NLM and SDI) and their impacts on dynamic behavior prediction.
4. To verify the effectiveness of the proposed models through comprehensive simulation and analysis, including static characteristic fitting and double pulse tests.
5. To establish a scientific basis for selecting appropriate modeling strategies for different power semiconductor devices based on their physical structures.

1.2 Research Questions

This research addresses several key questions in the field of power semiconductor device modeling:

1. How can the accuracy of IGBT models be improved in the low-voltage transition region while maintaining mathematical simplicity and physical reasonableness?
2. Why do MOSFETs and IGBTs respond differently to the same modeling correction methods, and what structural or physical mechanisms explain these differences?
3. How do carrier transport mechanisms and conductivity modulation in different device structures affect the effectiveness of model corrections?
4. What are the comparative advantages and limitations of different capacitance modeling methods (NLM vs. SDI) in representing dynamic behavior of power devices?
5. How can we effectively validate and quantify the improvements in model accuracy, particularly in critical operating regions?

By addressing these questions, this research aims to bridge the gap between physics-oriented and mathematics-oriented approaches to semiconductor device modeling, providing both theoretical insights and practical solutions for power electronics design.

1.3 Contribution

This research makes several significant contributions to the field of power semiconductor device modeling:

1. Development of a novel correction method based on transfer characteristics that significantly improves the fitting accuracy of IGBT models in the low-voltage region. The average fitting accuracy improved by 12.6% in the MATLAB environment and 21.7% in the circuit simulator, with improvements up to 77.9% under specific gate voltage conditions.
2. Quantitative analysis of the different responses of MOSFETs and IGBTs to the same correction method, revealing that IGBTs are significantly more sensitive to transfer characteristic corrections due to their composite structure and minority carrier injection mechanisms.
3. Comprehensive comparison of two major capacitance modeling methods (NLM and SDI), providing scientific basis for engineers to select the most appropriate implementation strategy for different application scenarios.
4. Verification of the physical reasonableness of the proposed corrections through analysis of the underlying carrier transport mechanisms and conductivity modulation processes in different device structures.
5. Development of a systematic testing framework combining static characteristic fitting analysis and dynamic double pulse testing, providing a robust validation methodology for power semiconductor device models.

These contributions not only enhance the accuracy of power semiconductor device models but also deepen the understanding of the physical mechanisms that underlie the different behaviors of MOSFETs and IGBTs, particularly in transition regions.

1.4 Structure of the Thesis

This thesis is organized into the following chapters:

Chapter 1: Introduction - Presents the aims and objectives, research questions, contributions, and overall structure of the thesis.

Chapter 2: Literature Review - Provides a comprehensive review of existing semiconductor device modeling methods, functions of models, challenges in modeling, and validation techniques. The chapter covers the evolution of MOSFET and IGBT modeling approaches, capacitance modeling methods, and identifies key research gaps.

Chapter 3: MOSFET and IGBT Model Correction and Analysis - Describes the methodology, including an overview of semiconductor device modeling approaches, the proposed correction method for the static part based on transfer characteristics, and the principles of different capacitance modeling methods for the dynamic part.

Chapter 4: Results and Analysis - Presents detailed experimental results, including comparative analysis of MOSFET and IGBT static model fitting, dynamic capacitance modeling test results, and double

pulse test results. The chapter includes comprehensive analysis of the improvement effects and explains the physical mechanisms behind the observed differences.

Chapter 5: Conclusions and Future Work - Summarizes the key findings, discusses their implications for power electronics design, and suggests directions for future research.

Each chapter builds upon the previous ones to provide a coherent narrative of the research, from the identification of the problem to the development and validation of the solution.

1.5 Summary

This chapter has introduced research on the correction and analysis of MOSFET and IGBT models, highlighting the importance of accurate modeling of semiconductor devices for power electronic systems. The aims and objectives focus on developing improved models that address the limitations of existing approaches, particularly in the low-voltage region of IGBTs. The research questions probe the underlying physical mechanisms that explain different responses to model corrections across device types.

The contributions of this research include a novel correction method that significantly improves IGBT model accuracy in critical operating regions, comprehensive comparison of capacitance modeling methods, and deeper understanding of the physical differences between MOSFETs and IGBTs. The thesis structure outlines how these contributions are developed and presented across the subsequent chapters.

This research bridges the gap between modeling approaches oriented to physics and oriented to mathematics, providing both theoretical insights and practical solutions that can enhance the design and simulation of power electronic systems. By improving the accuracy of semiconductor device models, particularly in transition regions, this work contributes to the advancement of power electronics technology in applications ranging from renewable energy systems to electric vehicles and industrial automation.

2 Literature Review

2.1 Functions of Semiconductor Device Models

2.1.1 Performance Prediction

Semiconductor models are crucial for predicting device behavior under different operating conditions, reducing the need for extensive physical testing. However, existing models face challenges in accuracy in high-temperature environments. Miyake et al. [2] pointed out that advanced IGBT models require comprehensive parameter extraction procedures that account for electrothermal characteristics to improve prediction accuracy in high-temperature scenarios. These limitations are particularly evident in high-power applications where heat dissipation and electrothermal coupling play key roles. Integrating temperature-sensitive parameters into compact models is essential to effectively address this gap.

2.1.2 Design Optimization

Compact models facilitate circuit design optimization through efficient simulation of losses and thermal behavior. Koziel et al. [3] demonstrated that surrogate-based modeling and optimization techniques can accurately predict thermal and electrical losses, helping engineers refine designs while reducing computational costs. However, sensitivity to parameter variations in complex systems remains an area that has not been explored enough, limiting the robustness and adaptability of the model. For example, variations in gate drive resistance and load conditions often lead to switching losses that cannot be accurately predicted, which existing compact models fail to fully capture.

2.1.3 Cost Reduction

Accurate modeling also contributes to a significant cost reduction by decreasing reliance on physical prototypes and failure testing. Islam et al. [4] developed artificial neural network models to predict the lifetime of semiconductor power devices under power cycle stress, which can reduce testing costs and accelerate development cycles, providing early insights into device reliability. When combined with external circuit test data, these AI-based models can further simplify the design process, reducing the costs associated with iterative hardware testing.

2.2 Basics of MOSFET and IGBT Modeling

2.2.1 Evolution of MOSFET Static Characteristics Modeling

MOSFET static characteristics modeling has undergone significant evolution, evolving from early simplified models to modern complex compact models. The Level 1 model [5] was the first widely used MOSFET model, employing a regional approximation approach to describe the behavior of MOS transistors. Subsequently, the Level 2 model [6] introduced the effects of carrier mobility variations with the electric field, improving the model accuracy in short-channel devices. The BSIM series models [7, 8]

further refined this direction, developing a more comprehensive framework that included the operation of the subthreshold region and the dependence of temperature.

The BSIM series models [7, 8], developed at UC Berkeley, represent a major advancement in MOSFET modeling, progressively increasing the physical precision and parameter complexity from BSIM1 to BSIM4. Modern power MOSFET modeling faces unique challenges, particularly in describing non-linear effects under high current and high voltage operating conditions. The MOSFET power model proposed by Hefner and Blackburn [9] pays special attention to accurately characterizing the variation of the resistance of the drain source (Rds * Rds *) with the drain current and temperature, which is critical for the prediction of power loss in high-frequency switching applications [9].

2.2.2 Development of Power MOSFET Models

The development of power MOSFET models highlights the evolution from traditional silicon-based devices to emerging wide bandgap semiconductor technologies. Early power MOSFET models focused mainly on static I-V characteristics, such as the model proposed by Kraus and Mattausch [10] in 1998. Over time, the focus of the research shifted towards accurately capturing switching transients and dynamic behavior, as exemplified by the model developed by McNutt and Hefner [11] that included non-linear capacitance and temperature effects.

The emergence of wide-bandgap semiconductor technologies, particularly silicon carbide (SiC) and gallium nitride (GaN) devices, has greatly driven the development of power MOSFET models. The compact model proposed by Chen [12] for SiC MOSFETs specifically addresses their unique physical characteristics, including the structure of the conduction band and variations in carrier mobility with temperature and electric field. Kaisheng et al. [13] further investigated the impact of non-linear capacitance characteristics in wide-band-gap power devices on switching losses, providing key insights for high-frequency application modeling.

Modern power MOSFET models increasingly emphasize the balance between physical mechanisms and practicality, a trend that evolved from early work such as the physics-based semiconductor models by Kraus et al. [10]. These developments provide a theoretical foundation and practical background for the application of the transfer characteristic correction method in this research.

2.2.3 IGBT Static Modeling Methods

Traditional IGBT static models belong to mathematically characteristic-oriented approaches inspired by physical properties, typically taking the following form:

$$I_{ST} = a - \frac{a}{1 + (V_{CE}/b)^c} \tag{2.1}$$

where I_{ST} is the collector current, V_{CE} is the collector-emitter voltage, and the parameters a, b, and c are functions related to the gate voltage V_{GE}. This model structure maintains mathematical simplicity while capturing the main physical characteristics of the IGBT, but it still faces challenges in a precise fitting in the low voltage region [14]. In circuit simulation environments, IGBTs are often implemented as hybrid equivalent circuits of N-channel MOSFETs and PNP bipolar transistors, reflecting the dual nature of their

internal physical structure.

2.2.4 Sechyp Model and Characteristic Decomposition

The Sechyp model adopts an approach to decomposing the characteristics of the device into the product of the transfer characteristics (F_{Trans}) and the output characteristics (F_{Out}), with its basic form as:

$$I_{DS} = F_{Trans}(V_{GS}) \cdot F_{Out}(V_{DS}) \tag{2.2}$$

This decomposition method provides a new perspective for understanding power semiconductor device behavior, particularly advantageous in analyzing nonlinear characteristics in transition regions. Wiedemann et al. [15] developed a reduced order modelling approach for IGBT modules, achieving accurate characterization of junction temperature based on the on-state resistance. Perez et al. [16] developed a unified Si/SiC IGBT model based on this idea, achieving accurate characterization of both N-channel and P-channel devices. Mihalic et al. [17] further explored the implementation of this method in the SPICE environment, providing feasible solutions for engineering applications.

2.2.5 Structural Differences Between IGBT and MOSFET

Understanding the basic structural differences between IGBT and MOSFET is crucial for accurate modeling. Huang et al. [18] demonstrated that IGBT employs a five-layer structure (emitter metal-N+ emitter region-P body region-N- drift region-P+ collector region-collector metal), while MOSFET uses a four-layer structure, resulting in significant differences in carrier transport mechanisms between the two. Baliga [19] described IGBT as having a dual modulation mechanism: on one hand, MOS channel control similar to MOSFET, and on the other hand, bipolar injection effects, with P+ collector region injecting minority carriers (holes) into the N drift region, reducing on-state resistance. This complex interaction between gate control and bipolar conduction explains why the same modeling methods may produce different effects between these two device types, especially in the transition region.

2.3 Major Challenges in Power Semiconductor Device Modeling

2.3.1 Low-Voltage Region Modeling Challenges

The nonlinear characteristics exhibited by power semiconductor devices in the low-voltage region have always been a challenge for accurate modeling.Liang et al. [20] proposed an improved analytical model, specifically optimized for predicting the switching performance of power semiconductor devices, significantly improving the modeling accuracy in critical operating regions. Verneau et al. [21] established a physics-based description method for low-voltage region conduction characteristics by analyzing the internal carrier distribution of power MOSFETs, providing a theoretical basis to accurately capture transition region characteristics. These studies indicate that low-voltage region modeling requires special mathematical treatment and physical understanding, especially for composite structure devices such as IGBTs, whose behavior in this region is more complex and requires comprehensive consideration of the coupling effects of multiple physical effects.

2.3.2 Carrier Transport Mechanisms

2.3.3 Carrier Transport Mechanisms

The fundamental differences in carrier transport mechanisms between MOSFETs and IGBTs create distinctly different modeling challenges. Baliga [22] in his authoritative work elaborates that MOSFETs rely solely on majority carrier (electron) conduction, with carrier type remaining unchanged as current flows from drain to source, while IGBTs involve a more complex dual-carrier transport mechanism. Trivedi and Shenai [23] described in detail the process in IGBTs where electrons flow from the N+ emitter region into the P body region to form an inversion layer (channel), then continue to flow through the N- drift region to reach the P+ collector region, while the P+ collector region injects minority carriers (holes) into the N drift region. This dual-carrier mechanism creates what Baliga [22] terms an ”electron-hole plasma region,” significantly altering the internal field distribution and making the mathematical description of current-voltage characteristics more complex. By injecting minority carriers (holes) from the collector p+ region into the n- drift region during forward conduction, the resistance of the n- drift region is considerably reduced Insulated-gate bipolar transistor - Wikipedia, but as Baliga [22] further explains, this advantage comes with additional complexity in switching behavior and device modeling.

2.3.4 Dynamic and High-Power Application Challenges

Compact models often struggle to accurately predict dynamic responses such as di/dt and dv/dt, especially in extreme operating conditions where high injection levels and fast transition effects become prominent. Yang et al. [24] developed an improved behavioral model for high-voltage and high-power IGBT chips that addresses these challenges by incorporating nonlinear dynamic effects observed in extreme operating conditions. These challenges are further exacerbated by external circuit characteristics, including gate drive resistance, parasitic inductance, and load variations, which introduce additional complexity to device behavior. Jeong et al. [25] demonstrated that ANN-based compact models with expandable parameter extraction techniques for emerging transistors can improve dynamic parameter calibration, providing a way to enhance the accuracy and reliability of compact models in capturing real-world interactions and dynamic phenomena.

2.3.5 Parameter Extraction Challenges

A key potential limitation of compact models lies in the complexity and time-consuming nature of parameter extraction, which is crucial for ensuring that models accurately reflect device behavior under different operating conditions. Compact models rely on parameters precisely calibrated through detailed analysis and iterative processes, often requiring extensive expertise and significant computational effort. For example, Navarro et al. [26] developed a sequential model parameter extraction technique for physics-based IGBT compact models, demonstrating the intricate steps required to properly characterize device behavior from various operating regions. This structural approach helps address the complexity challenge, but still requires expertise to implement effectively. This bottleneck is particularly problematic in fast-paced design environments where rapid prototyping, quick adaptation to new devices, and iterative testing are essential for maintaining competitiveness, highlighting the need for more efficient and automated parameter extraction methods.

2.4 Capacitance Modeling Methods and Implementation

2.4.1 Capacitance Model Selection

Selecting appropriate capacitance models for power semiconductor devices requires careful consideration of available data sources and computational efficiency. Nelson et al. [1] identified three main approaches in the literature: piecewise functions, continuous functions, and lookup tables (LUTs). While piecewise functions provide high fitting accuracy, they may introduce convergence problems. Continuous functions (such as arctangent, exponential, or hyperbolic tangent) ensure continuous differentiability but typically require numerous fitting parameters. As described by Mukunoki et al. [27], LUTs are popular due to their ability to be directly implemented from measurement data and their simplicity. For manufacturer datasheets providing limited characteristic points, continuous functions can achieve smooth interpolation between measurement points and facilitate parameter adjustment and sensitivity analysis [28]. In contrast, TCAD simulations typically generate a large number of data points already containing rich physical information and smoothness, making the LUT method applicable without the need to develop complex mathematical models [29].

2.4.2 Nonlinear Mapping Method (NLM)

2.4.3 Nonlinear Mapping Method (NLM) Implementation Approaches

The Nonlinear Mapping Method (NLM) has been implemented through several distinct approaches in semiconductor device simulation. Zeltser and Ben-Yaakov [30] proposed a comprehensive framework distinguishing between "total capacitance" ($C_t(v) = Q/v$) and "local capacitance" ($C_d(v) = dQ/dv$), implementing these concepts through a circuit-based technique using behavioral sources in SPICE. Their approach establishes a mathematical foundation by representing the nonlinear capacitance as $Q = \int C_d(v)dv$ and applying symbolic differentiation to avoid numerical instabilities. Duan et al. [31], meanwhile, developed a specialized implementation for SiC power MOSFETs by modeling junction capacitances through piecewise equations aligned with measured device characteristics. Their method incorporates a voltage-dependent hybrid formulation where $C_{gd}(v_{gd})$ and $C_{gs}(v_{gs})$ are expressed as continuous functions derived from physics-based parameters and fitted to experimental data. This technique excels in predicting switching behavior under high-frequency operation by accurately capturing the dynamic response of depletion regions across the entire operating voltage range while maintaining superior numerical stability during complex circuit simulations.

2.4.4 Simple Derivative Implementation Method (SDI)

The Simple Derivative Implementation Method (SDI) provides a direct and intuitive approach to simulating voltage-dependent capacitance, implementing the basic capacitor current equation $I = C(v) \cdot dv/dt$ directly through a behavioral current source. Nelson et al. [1] analyzed two main variants: SDI1 for capacitance definition implementation (current source expression $I = C_0 \cdot f_c(V_{1,2}) \cdot d/dt(V_{1,2})$, where f_c is the voltage-dependent capacitance function) and SDI2 for charge definition implementation (simplified expression $I = d/dt(f_q(V_{1,2}))$, where f_q is the voltage-dependent charge function). While SDI provides conceptual simplicity and direct correspondence with physical definitions, Nelson's comparative analysis

revealed a key limitation: its accuracy is highly dependent on the simulation time step selection. Their experiments clearly demonstrated that as the maximum time step decreases, the SDI prediction of damping characteristics gradually approaches the theoretically correct NLM prediction results, implying that extremely small simulation time steps need to be adopted to achieve acceptable accuracy, significantly increasing the computational burden.

2.5 Model Validation Methods

2.5.1 Double Pulse Test Dynamic Characterization

The Double Pulse Test (DPT) has become the industry standard method for evaluating the switching characteristics and losses of power semiconductor devices. Meisser et al. [32] focused on integrated SiC MOSFET modules with ultra-low parasitic inductance design, providing a critical experimental foundation for noise-free ultra high speed switching evaluation. Hoene et al. [33] developed ultra-low-inductance power module designs specifically optimized for fast switching semiconductors, demonstrating significant improvements in switching performance and measurement accuracy. Nayak et al. [34] conducted a comprehensive comparative study of different loss measurement techniques for SiC MOSFET based power converters, including double pulse test (DPT) and calorimetric methods for switching loss estimation.

2.5.2 EMI and Switching Characteristics Correlation

Electromagnetic interference (EMI) assessment has become a key aspect of power device model validation, with capacitance modeling methods significantly influencing prediction accuracy. Wang et al. [35] demonstrated the decisive role of accurate capacitance models in predicting switching ringing and high-frequency noise, particularly studying how parasitic elements affect MOSFET switching performance. Haleem et al. [36] provided empirical evidence for capacitance model selection by comparing IGBT switching transient characteristics under different circuit topologies. Dwiza et al. [37] further verified the significant impact of capacitance models on system-level EMI performance through analytical approaches for common mode noise analysis in power converters. These studies collectively indicate that different capacitance implementation methods (NLM vs. SDI) may produce notably different results in EMI prediction, with NLM methods typically providing better curve smoothness and integral calculation stability, suitable for system-level simulation, while SDI methods may more accurately capture transient peak losses and critical state characteristics under edge operating conditions.

2.5.3 Parameter Extraction and Validation Methods

2.5.3.1 Curve Fitting Methods

Traditional methods, such as least squares optimization, are widely applied in parameter extraction due to their simplicity and computational efficiency. Navarro et al. [26] developed a sequential model parameter extraction technique for physics-based IGBT compact models that provides a systematic approach to calibrating parameters from different operating regions. This approach has proven effective for static and linear operating conditions. However, when applied to scenarios involving complex nonlinear behavior

or rapid dynamic transitions, these methods face significant challenges where assumptions of linearity and stability are broken, resulting in reduced accuracy and limited applicability in high-frequency or high-power systems.

2.5.3.2 Machine Learning Methods

Machine learning offers powerful and robust alternatives for parameter extraction, especially in complex systems where traditional methods struggle to handle nonlinearity and dynamic behavior. Guo et al. [38] introduced an end-to-end AI-based automated process for semiconductor device parameter extraction that significantly reduces the need for manual adjustments while enhancing the model's ability to adapt to different operating conditions. These data-driven approaches are particularly effective at capturing complex relationships between variables, achieving higher accuracy and efficiency. However, they also present challenges such as the need for extensive training datasets to ensure model reliability and the enormous computational resources for processing and optimization, which may limit their accessibility and scalability in certain design environments.

2.5.3.3 Hybrid Methods and Future Automation

Hybrid methods combine the strengths of traditional approaches and machine learning techniques, achieving a balance between accuracy and computational efficiency. Duong et al. [39] demonstrated the effectiveness of physics-based compact model parameter extraction and optimization for GaN HEMTs, achieving significant improvements in dynamic and thermal modeling accuracy. Similarly, Miyake et al. [2] proposed a comprehensive parameter extraction procedure for advanced IGBT models with electro-thermal features, employing iterative optimization particularly effective in calibrating dynamic parameters. These hybrid methods show tremendous potential in leveraging external circuit test data, which can further enhance parameter accuracy by capturing real-world interactions and conditions.

2.6 Research Directions and Opportunities

Based on this literature review, we can identify several key research directions closely related to the model developed in this paper:

1. **IGBT Low-Voltage Region Characteristic Modeling**: For the nonlinear behavior in the low-voltage region caused by the complex physical structure of IGBTs, more accurate mathematical models and physical interpretations need to be developed, with special attention to the interaction between minority carrier injection and gate control.
2. **Capacitance Modeling Method Optimization**: Further explore the performance differences between NLM and SDI methods under different operating conditions, and develop improved implementation schemes that balance numerical stability and computational efficiency.
3. **Extension of Transfer Characteristic Correction Method**: Extend the transfer characteristic correction method developed in this research to other power semiconductor devices, studying its applicability and effectiveness in different device structures and material systems.

4. **Improvement of Model Validation Techniques**: Refine the double pulse test method, closely integrating it with EMI prediction to establish a more comprehensive power device model validation framework.
5. **Integration of Model-Based and Data-Driven Approaches**: As demonstrated by Zhang et al. [40], combining model-based and data-driven methods for remaining useful life prediction of power MOSFETs provides improved accuracy and reliability. This hybrid approach represents a promising direction for enhancing both modeling accuracy and practical applicability.

These research directions will help improve the accuracy and practicality of power semiconductor device models, especially in system-level simulation and high-performance applications. graphicx

3 MOSFET and IGBT Model Correction and Analysis

3.1 Overview of Semiconductor Device Modeling Methods and Research Data Sources and Experimental Design

Two main methodological schools have long existed in the field of power semiconductor device modeling: physics-oriented and mathematics-oriented approaches. These two methods have their own characteristics in model construction, parameter selection, and application scenarios, with far-reaching impacts on subsequent research.

The physics-oriented approach provides an intuitive conceptual model that corresponds directly to the physical structure of semiconductor devices. This method provides clear physical interpretations for each functional component, making the parameters easy to understand from a theoretical perspective, with predictable effects when adjusted. Each part of the equation represents a specific physical phenomenon within the device, such as the transfer characteristic function that simulates the control of the MOS channel, while the output characteristic function captures bipolar transistor behavior. This direct physical mapping makes the model particularly suitable for research and development work that requires in-depth understanding of the physics of the device and its working mechanisms.

In contrast, the mathematics-oriented approach, while more abstract in its conceptual model, establishes meaningful connections with physical characteristics through its hierarchical parameter structure. The physical meaning of parameters is more indirect, relying more on numerical fitting results and empirical knowledge. Parameter effects are more difficult to predict intuitively and require experience to interpret. However, this abstraction brings significant advantages in computational performance for complex systems. The relationship between mathematical formulas and device behavior is reflected through careful adjustment of parameters rather than explicit physical representation. This approach performs excellently in practical engineering applications, especially in cases where computational efficiency takes precedence over theoretical analysis, providing reliable performance in system-level simulation.

In terms of implementation complexity and software compatibility, physics-oriented equation implementation requires handling complex mathematical functions, with more cumbersome computational processes, and may require developers to custom-implement special functions, increasing the difficulty of cross-platform migration. Mathematical-oriented equations, on the other hand, rely only on basic mathematical operations, with standard support in all mainstream SPICE-type simulation tools, greatly reducing implementation difficulty and maintenance costs.

Convergence is a key factor in circuit simulation, directly affecting the reliability and computational efficiency of the results. The complex mathematical structure of physics-oriented equations, while accurately describing device behavior, may lead to a reduced convergence speed, especially with potential numerical instability in certain operating areas. Mathematical-oriented equations, with their concise mathematical structure, typically exhibit superior convergence properties, performing more robustly in complex system simulations.

In practical applications, the ideal strategy often combines the strengths of both approaches: using mathematics-oriented equations for preliminary system design and large-scale simulation stages, and transitioning to physics-oriented equations for detailed analysis of key components and studies of extreme operating conditions. This chapter will systematically analyze the application of these two methods in MOSFET and IGBT modeling, exploring how to maintain the physical reasonableness of the model while improving its numerical efficiency and practicality.

The objective of this research is to create accurate and portable wide-bandgap semiconductor SPICE behavioral models. The research data comes from two main sources: MOSFET data from WOLFSPEED's C2M0080120D device, and IGBT data based on simulated data points provided by TCAD physical models.

The WOLFSPEED C2M0080120D was chosen as the MOSFET research subject because it represents the main applications of modern wideband gap semiconductor technology, with typical characteristics and challenges. The experimental platform uses the open-source software LTspice, chosen based on two considerations: first, its open-source nature makes research results easily accessible; second, its compatibility allows models to be conveniently transferred to other SPICE software platforms, enhancing the application value of the research results.

Note that during the experiment, slight differences were found between the MOSFET device test results in the SPICE model and the datasheet. This difference may originate from system bias between WOLFSPEED's hardware testing equipment and SPICE simulation software. To ensure consistency and comparability of the research, this study chose the simulation results of the device model in SPICE as the benchmark comparison object, rather than directly using datasheet data.

For the IGBT modeling part, the research data comes from exact data points generated by TCAD (Technology Computer-Aided Design) physical models. These data points, calculated on the basis of semiconductor physical equations and detailed device structural parameters, have high physical accuracy and can reflect microscopic physical processes such as carrier distribution and electric field distribution within the IGBT. The data provided by TCAD models covers static characteristics under different gate voltages and collector voltages, providing a reliable foundation for developing high-precision IGBT behavioral models.

This dual source approach effectively eliminates systematic errors between different platforms, making the effects of model improvement more objective and credible, while also facilitating comparison of performance differences between MOSFET and IGBT under the same modeling method.

3.2 Static and Dynamic Modeling of Semiconductor Devices

3.2.1 Static Part of Semiconductor Device Model

3.2.1.1 Overview of Traditional IGBT Static Model

The IGBT (Insulated Gate Bipolar Transistor), as a key device in modern power electronic systems, requires precise modeling for system design and simulation. The traditional IGBT static model belongs to the mathematics-oriented approach inspired by physical properties, typically taking the following form:

$$I_{ST} = a - \frac{a}{1 + (V_{CE}/b)^c} \tag{3.1}$$

Where I_{ST} is the collector current, V_{CE} is the collector-emitter voltage, and the parameters a, b, and c are functions related to the gate voltage V_{GE}:

$$a = \frac{s1_a}{1 + ((V_{GE} - V_{th})/s2_a)^{s3_a}} + s4_a \tag{3.2}$$

$$b = \frac{s1_b}{1 + ((V_{GE} - V_{th})/s2_b)^{s3_b}} + s4_b \tag{3.3}$$

$$c = \frac{s1_c}{1 + ((V_{GE} - V_{th})/s2_c)^{s3_c}} + s4_c \tag{3.4}$$

This model form is concise and mathematically clear: parameter a represents the maximum current value, parameter b controls the position of the transition point from the linear region to the saturation region, and parameter c determines the steepness of the transition region. This model form originally originated from static modeling of MOSFETs and was later successfully applied to IGBTs, but still faces certain challenges in accurately fitting IGBT characteristics, especially the transition characteristics in the low V_{CE} region.

In circuit simulation environments, IGBTs are often implemented as hybrid equivalent circuits composed of N-channel MOSFETs and PNP bipolar transistors. This representation reflects the dual nature of the internal physical structure of IGBTs: the combination of MOS channel control and bipolar conduction mechanisms. In the low-voltage region, IGBT behavior is mainly influenced by channel formation and modulation, while in the high-voltage region it exhibits more characteristics of bipolar devices. This dual nature makes precise modeling of IGBTs more challenging than single devices. This is also the main reason why this model form faces challenges in accurately fitting transition characteristics in the low V_{CE} region.

In subsequent sections, we will propose an improved model that can more accurately describe the behavior of the transition region through corrections to transfer characteristics based on the traditional static model. This modification maintains the simplicity and physical meaning of the model while significantly improving its prediction accuracy in the low-voltage region.

3.2.1.2 Transfer Characteristics and Output Characteristics Decomposition of Sechyp Model

In exploring more effective IGBT modeling methods, we were inspired by the MOSFET Sechyp model. The Sechyp model, which belongs to the physics-oriented approach, adopts a unique method: decomposing the device characteristics into the product of the transfer characteristics (F_Trans) and the output characteristics (F_Out).

The basic form of the Sechyp model is as follows:

$$I_{DS} = F_{Trans}(V_{GS}) \cdot F_{Out}(V_{DS}) \tag{3.5}$$

Here F_{Trans} mainly describes the modulation effect of the gate voltage on current and F_{Out} describes the influence of drain voltage on current. This decomposition method provides a new perspective for understanding semiconductor device behavior, especially when analyzing transitional regions.

Further analyzing the traditional IGBT model $I_{ST} = a - \frac{a}{1+(V_{CE}/b)^c}$, we can rewrite it as:

$$I_{ST} = a \cdot \left(1 - \frac{1}{1 + (V_{CE}/b)^c}\right) \tag{3.6}$$

At first glance, this mathematical transformation seems to suggest that the parameter a corresponds to $F_{Trans}(V_{GE})$, and the expression $\left(1 - \frac{1}{1+(V_{CE}/b)^c}\right)$ corresponds to $F_{Out}(V_{CE})$. However, this simple correspondence has a key issue: in the traditional IGBT model, the parameters a, b, and c are all functions of V_{GE}, making the correspondence more complex.

In fact, a more accurate physical interpretation should be: parameter a mainly controls the current magnitude in the saturation region; From a physical meaning perspective, it is closer to the part describing output characteristics, that is, the maximum current the device can reach at a specific gate voltage; parameters b and c control the transition characteristics from linear region to saturation region; from a physical meaning perspective, they are closer to transfer characteristics, as they describe how gate voltage modulates the channel.

Based on insights from the Sechyp model, we recognize that IGBT transfer characteristics should be influenced by both V_{GE} and V_{CE}. This means that to establish a more accurate IGBT model, the parameters b and c should not only be functions of V_{GE} but should also consider the influence of V_{CE}. Similarly, from a physical perspective, there exists a complex interaction between the gate voltage (V_{GE}) and the collector voltage (V_{CE}), especially in the transition region.

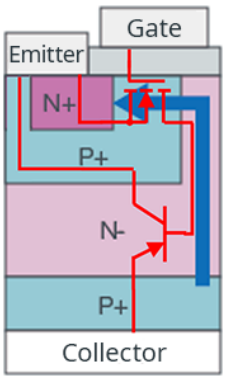
This understanding provides a new approach to develop improved IGBT models: By introducing corrections based on transfer characteristics in parameters b and c, while considering the interaction between V_{GE} and V_{CE}, we can more accurately capture the behavioral characteristics of IGBTs in the transition region. This approach is particularly suitable for IGBTs, as their composite structure and the presence of minority carriers make the interaction between gate control and collector voltage more significant.

3.2.1.3 Analysis of Structural Differences Between IGBT and MOSFET

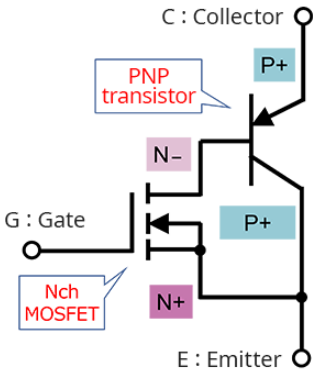
IGBT and MOSFET have fundamental differences in semiconductor physical structure, which directly affect their sensitivity to model corrections. As shown in Figure 3.1, the IGBT is essentially a composite structure of a MOSFET and a bipolar junction transistor (BJT), with an additional collector region P+, which introduces minority carrier injection mechanisms.

Structurally, MOSFETs adopt a four-layer structure (source metal-N+ source region-P body region-N-drift region-N+ substrate-drain metal), while IGBTs adopt a five-layer structure (emitter metal-N+ emitter region-P body region-N-drift region-P+ collector region-collector metal). This additional P+ layer creates a PNP bipolar transistor structure, forming a composite working mechanism with the MOS control channel.

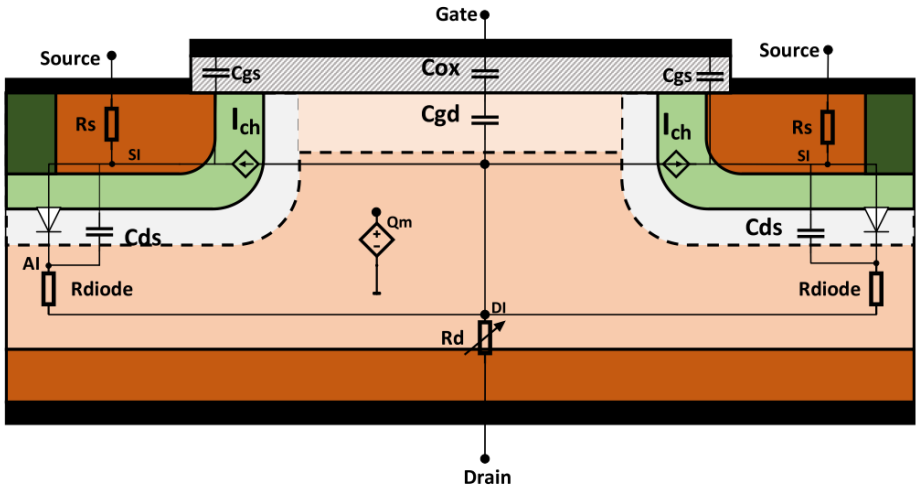
This structural difference leads to more complex transfer characteristics in IGBTs compared to MOSFETs, involving dual modulation mechanisms. MOS channel control (similarly to MOSFETs, the input part of



(a)



(b)



(c)

Figure 3.1: Comparison of IGBT and MOSFET structures. (a) The physical structure of IGBT. (b) The equivalent circuit of IGBT. (c) Cross-sectional structure of a MOSFET that relies solely on majority carrier conduction.

IGBTs is controlled by gate voltage to form channels, determining the switching state of the device) and bipolar injection effects (unlike MOSFETs, the output part of IGBTs includes a PNP structure, with the P+ collector region injecting minority carriers (holes) into the N-drift region, reducing on-resistance).

It is precisely this dual mechanism that gives IGBTs lower on-state voltage drop compared to MOSFETs in the conduction state, but also brings more complex current conduction and control characteristics. Our experimental results verified this: the same correction parameters can significantly improve the transition region fitting accuracy in IGBTs, while having a limited effect in MOSFETs. This indicates that the physical structure of IGBTs is more sensitive to transfer characteristic corrections, especially in the transition region.

IGBT and MOSFET have essential differences in carrier transport mechanisms, which is the key factor in their different responses to transfer characteristic corrections. There are significant differences in the flow path and the nature of the carriers in the two types of devices. MOSFETs are based solely on majority carriers (electrons) for conduction, and the type of carrier does not change as the current flows from the drain to the source. This single-carrier conduction mechanism makes its mathematical description relatively simple, with current-voltage characteristics mainly determined by channel electron concentration and mobility.

In contrast, IGBTs involve dual conduction of electrons and holes, forming complex carrier loops: electrons flow from the N+ emitter region into the inversion layer (channel) formed in the P body region; these electrons then continue flowing through the N-drift region to reach the P+ collector region, while the P+ collector region injects holes (minority carriers) into the N-drift region. Some of these injected holes flow towards the N+ emitter region through the P body region, while others recombine with electrons in the N-drift region, constituting the unique charge transport mechanism of IGBTs. In IGBTs, although the minority carriers (holes) injected from the P+ collector region are mainly controlled by V_{CE}, their distribution and effects in the drift region are influenced by the MOS channel electron flow (controlled by V_{GE}), forming a typical ”electron-hole plasma” region.

It should be noted that although minority carriers are mainly injected by drive V_{CE}, their presence significantly changes the distribution of the electric field and the distribution of conductivity within the device, thereby affecting the control efficiency of the gate in the channel. This influence is particularly significant in the low V_{CE} region: the injection and distribution of holes directly affect the electric field gradient, causing the transport characteristics of channel electrons to exhibit strong nonlinearity. This complex interaction makes it difficult to completely separate the ”transfer characteristics” from the ”output characteristics” in IGBTs, as there exists a strong coupling relationship between them. Therefore, corrections based on transfer characteristics can simultaneously affect multiple physical processes in IGBTs, producing more significant overall improvement effects.

IGBT and MOSFET also have significant differences in the conductivity modulation mechanisms, which further explains the different responses of the two devices to transfer characteristic corrections. There are essential differences in the conductivity formation and modulation processes of the two devices. In MOSFETs, conductivity is mainly directly controlled by the gate with a relatively simple mathematical expression:

$$G_{MOSFET} \approx \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{th}) \tag{3.7}$$

Where μ_n is the mobility of the electrons, C_{ox} is the capacitance of gate oxide, and W/L is the width to length ratio. This relationship indicates that MOSFET conductivity is mainly linearly modulated by gate-source voltage, with relatively simple channel formation and modulation processes.

In IGBT, the total conductivity consists of two parts:

$$G_{IGBT} \approx G_{MOS} + G_{drift}(n, p) \tag{3.8}$$

The MOS part (G_{MOS}) is similar to the MOSFET conductivity, while the drift region conductivity (G_{drift}) strongly depends on the concentration distribution of electrons and holes, exhibiting obvious nonlinear characteristics. Especially in the transition region, the injected holes significantly change the conductivity distribution in the drift region. This change in conductivity, in turn, affects the sensitivity of the channel current to V_{CE}, forming a complex feedback mechanism.

Based on the theoretical analysis presented above, we expect that the same transfer characteristic correction method will exhibit a significantly better performance improvement in IGBTs than in MOSFETs, especially in the low V_{CE} region. This is because: the composite structure of IGBTs makes the relationship between transfer characteristics and V_{CE} more nonlinear; the complex electric field distribution caused by minority carrier injection enhances parameter sensitivity; the dual conductivity modulation mechanism means that correction effects can simultaneously influence multiple physical processes. This theoretical expectation will be verified and quantitatively analyzed through detailed experimental results in Chapter 4.

3.2.1.4 IGBT Model Correction Method Based on Transfer Characteristics

3.2.1.4.1 Theoretical Basis of the Correction Method

Based on inspiration from the Sechyp model and analysis of IGBT physical characteristics, we propose a correction method based on transfer characteristics. The core concept of this method is: although the traditional model parameters b and c are formally functions of V_{GE}, their physical essence is closely related to the transfer characteristics and should consider the influence of both V_{GE} and V_{CE}.

From a physical perspective, IGBT behavior in the transition region is influenced by multiple factors: channel formation and modulation (as V_{CE} increases, the electric field near the channel end strengthens, causing the channel to gradually contract, directly affecting the control efficiency of the gate over the channel); minority carrier injection (although the minority carriers (holes) injected from the P+ collector region of the IGBT are mainly controlled by V_{CE}, their distribution in the drift region is influenced by the MOS channel electron flow (controlled by V_{GE}), forming complex interactions); and nonlinear changes in conductivity (the conductivity in the transition region exhibits strong nonlinear characteristics, which are difficult to describe solely through V_{GE} or V_{CE}). These physical phenomena indicate that, in the transition region, transfer characteristics have an inherent association with V_{CE}, requiring appropriate correction terms to capture this complex relationship.

3.2.1.4.2 Design and Implementation of Correction Functions

Based on the theoretical analysis described above, we designed correction functions for the parameters b and c, and implemented a complete enhanced IGBT model. The complete implementation of the enhanced model includes three key correction parts:

(1) Exponential decay correction for parameter b

$$b\_correction = k_b \cdot \exp(-\alpha_b \cdot V_{CE}) \tag{3.9}$$

$$b = b\_original \cdot (1 + b\_correction) \tag{3.10}$$

The correction for parameter b adopts an exponential decay function with the following characteristics:

$$b\_correction = k_b \cdot \exp(-\alpha_b \cdot V_{CE}) \tag{3.11}$$

$$b = b\_original \cdot (1 + b\_correction) \tag{3.12}$$

The parameter b in the traditional model controls the position of the transition point from the linear region to the saturation region, corresponding to the modulation effect of the channel length. The exponential decay correction makes b significantly larger in the low V_{CE} region, consistent with the special physical behavior of channel formation in the low-voltage region. Using a multiplicative combination $(1 + b_{correction})$ ensures that b always remains positive, avoiding numerical instability. At the same time, the multiplicative form makes the correction effect proportional to the original parameter, maintaining the physical continuity of the model. Through the parameters k_b (correction intensity) and α_b (decay rate), the degree of influence of the correction in different V_{CE} regions can be precisely controlled.

(2) Correction of the S-shaped function for the parameter c

$$c\_correction = k_c \cdot \left(1 - \frac{1}{1 + \exp(-\alpha_c \cdot (V_{CE} - \beta_c))}\right) \tag{3.13}$$

$$c = c\_original + c\_correction \tag{3.14}$$

The correction for parameter c adopts an S-shaped function with significant advantages for model optimization. The parameter c controls the steepness of the current-voltage curve, directly affecting the nonlinear characteristics of the transition region. The S-shaped function can produce rapid changes near specific V_{CE} values (β_c), precisely controlling the shape characteristics of the transition region. Unlike b, c adopts an additive combination, allowing more direct control of the changes in absolute values in c, achieving a more precise adjustment of the shape of the curve. Through parameters k_c (correction amplitude), α_c (steepness), and β_c (center position), a highly flexible control capability is provided, adapting to different working conditions.

(3) Supplementary correction for the linear region

$$linear\_term = linear\_coef \cdot V_{CE} \cdot \exp(-5 \cdot V_{CE}) \tag{3.15}$$

This additional linear correction term is specifically designed for extremely low V_{CE} regions (mainly <1.5V). The exponential decay factor ensures that the correction is effective only in the low V_{CE} region, not affecting the fitting in high-voltage regions. In extremely low-voltage regions, IGBTs often exhibit characteristics closer to linear, and this correction term directly simulates this behavior. Using a single parameter $linear\_coef$, the intensity of this correction can be easily controlled, providing a simple yet effective means of fine-tuning the model's performance in this critical operating region.

3.2.1.4.3 Physical Interpretation of the Correction Method

1. Correction of parameter b and channel modulation: In IGBTs, as V_{CE} increases, the enhancement of the electric field near the drain causes a reduction in channel length, an effect known as channel length modulation. The exponential decay correction of parameter b precisely captures this physical process: in the low V_{CE} region, the correction is strongest, reflecting the initial stage of channel formation; as V_{CE} increases, the correction gradually weakens, corresponding to the stabilization of the modulation effect of channel length.

2. Correction of parameter c and non-linear conduction characteristics: The nonlinear conduction characteristics of IGBTs are influenced by multiple factors, including drift-region resistance, space charge region width changes, etc. The correction of the S-shaped function of the parameter c reflects the concentrated manifestation of these factors within a specific range V_{CE}, especially in the middle section of the transition region, where nonlinearity is highest.

3. Linear correction term and initial conduction behavior: In extremely low V_{CE} regions, the initial conduction behavior of IGBTs often exhibits quasi-linear characteristics, which may come from contributions such as diffusion current at the PN junction edges. The linear correction term directly simulates this behavior, ensuring that the model maintains accuracy throughout the full voltage range.

Through these corrections, our model can significantly improve the fitting accuracy of IGBTs in the transition region based on physical reasonableness, providing a solid foundation for high-precision simulation of power electronic systems.

3.2.1.5 Static Part Test Circuit Setup

1. Reference MOSFET module C2M0080120D static test circuit: (Note: the source terminal is used as the ground terminal.)

The test circuit shown in Figure3.2 is specifically designed to measure the static characteristics of MOSFETs, with reasonableness reflected in multiple aspects. The circuit provides precise and stable test conditions through independent voltage sources of Vgs (20V) and Vds (10V), allowing gate and drain voltages to be controlled separately, thereby capturing complete device characteristics from the linear region to the saturation region. The VT voltage source (25V) connected to Tj (junction temperature) and Tc (case temperature) in the circuit is used to simulate or control the device temperature, ensuring

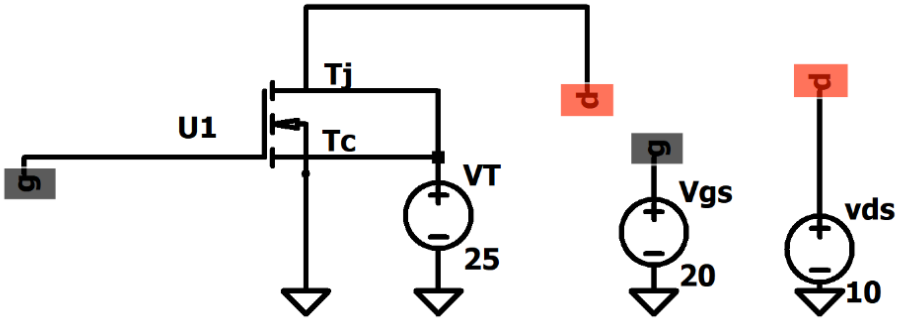
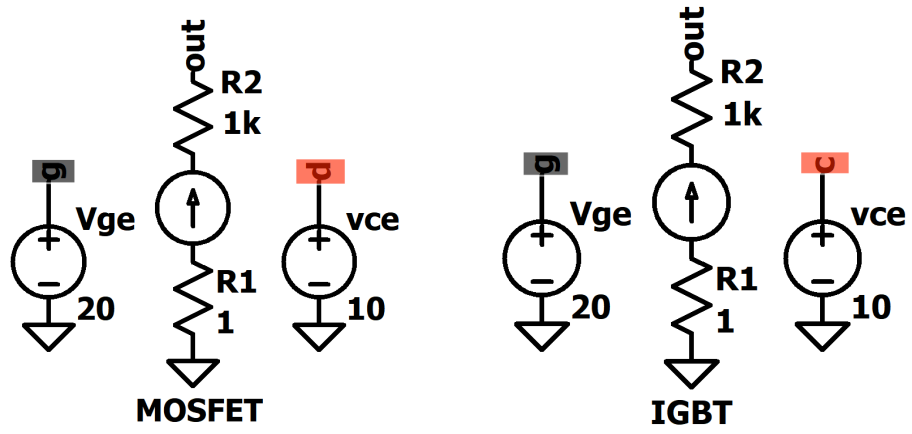


Figure 3.2: C2M0080120D static test circuit



(a) (b)

Figure 3.3: Application of static test for MOSFETs and IGBTs: (a) MOSFET static test circuit and (b) IGBT static test circuit

measurements under known stable temperature conditions. This measurement setup is directly related to the MOSFET static model formula discussed earlier:

$$I_{ds} = a(V_{gs}) \cdot \left[1 - \frac{1}{1 + (V_{ds}/b(V_{gs}))^{c(V_{gs})}}\right] \tag{3.16}$$

enabling complete output characteristic curve families to be obtained by scanning Vds at different Vgs values, for accurate extraction of model parameters a(Vgs), b(Vgs) and c(Vgs). This isolated measurement method not only ensures that measurements are not influenced by other circuit elements but also ensures measurement repeatability through precise control of each parameter while minimizing interference from wiring resistance and other parasitic effects. Therefore, this test method can obtain high-quality data covering all operating regions, providing data sources for the subsequent fitting and simulation of the MOSFET model.

Based on experimental verification of the static characteristics of commercial silicon carbide MOSFET device C2M0080120D, this research established a generalized power semiconductor device static characteristic test platform. As shown in Figure 3.4(a), this approach was successfully applied to testing the

static characteristics of MOSFETs, demonstrating the adaptability of the methodology. The test system uses behavioral current sources (B sources) as core modeling elements, supplemented by precise measurement networks (R1=1Ω, R2=1kΩ), achieving high-precision mapping from control signals to output characteristics.B sources demonstrate significant technical advantages in semiconductor device modeling: they support arbitrarily complex mathematical function expressions, accurately describing nonlinear model equations $I_{DS} = a(V_{GS})[1 - 1/(1 + (V_{DS}/b(V_{GS}))^{c(V_{GS})})]$; their multivariate control characteristics match the multiparameter dependency of power devices; built-in mathematical function libraries ensure smooth transitions between operating regions, significantly improving numerical stability; their parameterized structure facilitates model optimization and fitting.

For modeling the static characteristics of IGBTs, as shown in Figure 3.4(b) this research adopted the principle of structural similarity, maintaining the test circuit topology unchanged, only replacing node identifiers accordingly (G→G, D→C, S→E). The theoretical basis of this method lies in the isomorphic mathematical model framework of MOSFETs and IGBTs:

$$I = f(V_{control\ electrode})[1 - g(V_{main\ electrode}/h(V_{control\ electrode}))] \tag{3.17}$$

Notably, in the improvement of the IGBT model, by extending the original parameter functions $b(V_{GE})$ and $c(V_{GE})$ to $b(V_{GE}, V_{CE})$ and $c(V_{GE}, V_{CE})$, IGBT-specific physical phenomena such as minority carrier injection and complex conductivity modulation mechanisms were successfully captured. The introduction of such correction terms enables the model to accurately reflect the nonlinear behavior of IGBTs in the low V_{CE} region, while maintaining the consistency and computational efficiency of the implementation method. This behavior source-based modeling method provides a solid foundation for efficient simulation of power semiconductor devices, particularly suitable for parameter optimization and rapid prototype design of power electronic systems.

3.2.2 Dynamic Part of Semiconductor Device Model

3.2.2.1 Key Influencing Factors of Power Semiconductor Device Dynamic Characteristics

In power electronic system design, SPICE simulation tools are crucial for predicting system performance. For SiC MOSFET devices, their dynamic behavior is influenced by multiple factors, including conduction characteristics, switching characteristics, and parasitic parameters. However, according to Nelson et al. [1], when different SiC MOSFET models adopt the same inter-electrode capacitance model, their dynamic behavior differences significantly decrease. As shown in Figure 3.4, this result proves that the contribution of inter-electrode capacitance in dynamic behavior prediction is more substantial than the conduction branch. Therefore, the modeling of inter-electrode capacitance plays a critical role in SPICE simulation.

Nelson et al. [1] point out that there are two key issues in the literature regarding inter-electrode capacitance modeling for SiC MOSFETs. First is the choice of capacitance model: there are multiple capacitance description methods in the literature, including piecewise functions, continuous functions, and lookup tables (LUT). Piecewise functions, although having high fitting accuracy, may cause convergence problems according to research [1]; continuous functions (such as arctangent, exponential, hyperbolic tangent, etc.) guarantee continuous differentiability but are usually computationally complex and require

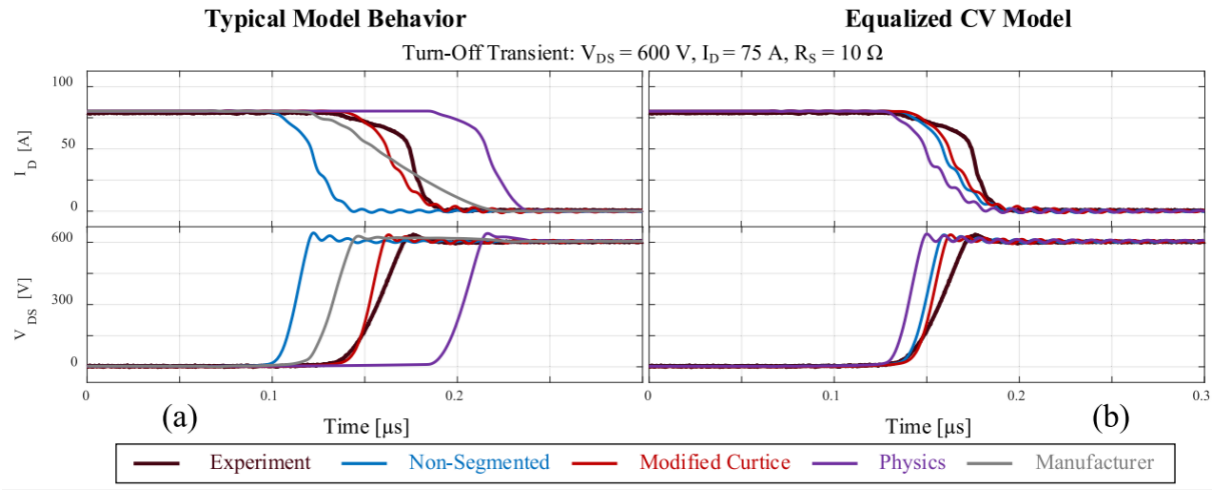


Figure 3.4: The influence of capacitance on dynamic behavior: Comparison between published models and experimental data for $R_g = 10\,\Omega$, $V_{DS} = 600\,V$, $I_D = 75A$, $T_j = 25°C$. (a) behavior as published in the literature, and (b) altered to have identical capacitance models. [Reproduced from [1]]

numerous fitting parameters; while the LUT method is widely applied in practical model development due to its "directly definable by measurement data" nature and simple implementation [41]. Second is how to implement these capacitance models in SPICE: even with a determined capacitance description method, there are multiple strategies for implementing these models in SPICE, directly affecting simulation accuracy and computational efficiency. As emphasized by Zeltser and Yaakov [30], "for voltage-dependent capacitances, different implementation methods may lead to significantly different simulation results and convergence performance, even if they are based on the same capacitance function." Therefore, for accurate and efficient SiC MOSFET dynamic simulation, not only is it necessary to select an appropriate capacitance model, but also to adopt a suitable SPICE implementation strategy.

In the field of power electronic device modeling, the main strategies for implementing voltage-dependent capacitances include total capacitance (CT) implementation, local capacitance (CD) implementation, nonlinear mapping method, simple derivative method, and charge-defined capacitor method, etc. [30]. Although the total capacitance (CT) implementation is conceptually intuitive, it often leads to convergence problems when dealing with nonlinear capacitances due to the capacitance derivative term in its current equation; the charge-defined capacitor (QDC) method establishes capacitance models by directly defining charge-voltage relationships, but not all SPICE versions support this feature.

This research particularly focuses on nonlinear mapping (NLM) and simple derivative implementation (SDI) methods, mainly based on the following considerations: first, these two methods have been widely applied in existing literature and have demonstrated good functionality; second, they represent two distinctly different implementation ideas—NLM achieves nonlinear characteristics through a combination of fixed linear capacitance and behavioral sources, while SDI directly uses differential equations and behavioral sources to describe capacitance current, making them ideal comparative research objects due to this methodological difference; finally, both methods can be applied to various capacitance models (piecewise functions, continuous functions, or LUT), providing good universality. According to research by Nelson et al. [1], the NLM method exhibits better numerical stability and computational efficiency,

especially in complex circuit simulations, while the SDI method, although simple to implement, has its accuracy heavily dependent on simulation time step length, a trade-off that needs careful consideration in practical applications. Through in-depth analysis of the performance of these two methods in SiC MOSFET simulation, scientific basis can be provided for power electronics design engineers to select the most appropriate implementation strategy, thereby optimizing simulation accuracy and efficiency.

3.2.2.2 Principles of LUT, NLM and SDI Methods

The Look-Up Table (LUT) method is a widely applied data-driven approach in power electronic device modeling. Its basic principle is to directly store discrete input-output correspondences, manifested in capacitance modeling as recording voltage-capacitance or voltage-charge pairs obtained from measurement or simulation. The LUT method can be directly defined by measurement data, thus avoiding the complex mathematical model derivation process. The LUT method is mainly divided into two implementation forms: capacitance-based LUT and charge-based LUT. Capacitance-based LUT directly stores discrete data points of voltage and corresponding capacitance values, calculating the corresponding capacitance value through interpolation algorithms (usually linear interpolation or spline interpolation) when encountering voltage values not present in the table during simulation; while charge-based LUT stores discrete data points of voltage and corresponding charge amounts, which, from a physical essence perspective, better conforms to the basic definition of capacitance (capacitance being the derivative of charge with respect to voltage), and may therefore have advantages in numerical stability. The prominent advantage of the LUT method lies in its ability to accurately reflect actual measurement data without presetting specific function forms, thus precisely capturing complex nonlinear capacitance characteristics common in wide-bandgap power devices. However, the accuracy of this method highly depends on the density and distribution of data points in the table, especially in rapidly changing voltage regions, which may require higher sampling density to ensure accuracy. Additionally, convergence problems caused by interpolation algorithms in some SPICE simulation environments still need attention. Overall, the LUT method provides an intuitive, efficient solution in voltage-dependent capacitance modeling, particularly suitable for developing power semiconductor device simulation models based on measured data.

The Nonlinear Mapping (NLM) method is an efficient SPICE simulation technique for implementing voltage-dependent capacitances, with its core idea being to transform complex nonlinear capacitance problems into a form combining linear capacitance with behavioral sources. Endruschat et al. [42] detailed the specific implementation method of NLM based on the work of Heckel and Frey [41]. The NLM method is implemented through a combination of multiple circuit elements: (1) fixed linear capacitance, using a constant capacitor C1 to perform differential operations; (2) behavioral current source, used for voltage-current mapping; (3) behavioral voltage source, mapping external voltage to internal nodes. The physical significance of this combination lies in: linear capacitance is responsible for handling time derivative calculations, while behavioral sources handle nonlinear mapping. Specifically, the NLM1 implementation contains the following element relationships: behavioral current source (Bi1): I = fc(V1,2) * Iv1; behavioral voltage source (Bv1): V = V1,2; fixed linear capacitance (C1): performing differential operations; voltage source (V1): V = 0. Here fc is the capacitance function, representing the relationship between capacitance value and voltage, which can be an analytical function or lookup table. From a circuit theory perspective, this implementation method cleverly utilizes the inherent time-domain

differential properties of linear capacitance, avoiding numerical errors brought by direct calculation of voltage derivatives in behavioral sources. In the method of Endruschat et al., through the introduction of auxiliary capacitance and control current sources, the current calculation expression is further optimized to is(t, vc) = iaux(t) · [C(vc)/Caux - 1], where iaux(t) is the current of the auxiliary capacitance, and C(vc) is the voltage-dependent capacitance function. This method not only has better numerical stability than the Simple Derivative Implementation (SDI), but also has significant advantages in computational efficiency, especially in accurately predicting system damping and oscillation characteristics without the need to reduce simulation time step size. The NLM method successfully transforms complex nonlinear differential equation problems into forms more amenable to numerical solution through clever combination of SPICE native elements and behavioral sources, providing reliable guarantees for efficient, high-precision simulation of power electronic systems.

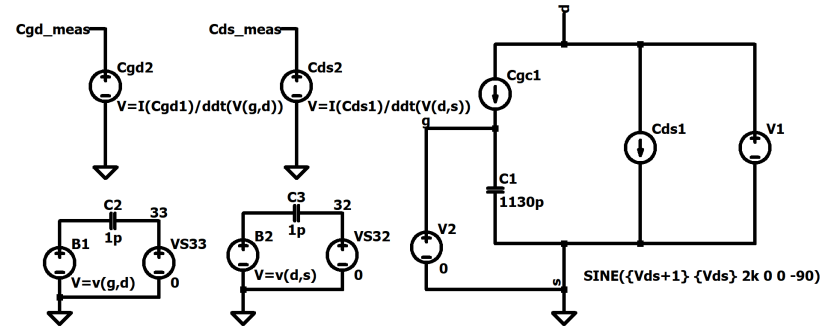
The Simple Derivative Implementation (SDI) method is a direct and intuitive voltage-dependent capacitance modeling technique, with its core idea being to directly construct the basic current equation of capacitance through a behavioral current source. Based on the classic physical formula of capacitance I = C(v) · dv/dt, the SDI method directly implements this relationship in the SPICE environment, without requiring additional circuit element combinations. Nelson et al. [1] analyzed in detail two main variants of SDI in their research: SDI1 and SDI2. SDI1 is mainly used for capacitance-defined implementation, as shown in Figure 3(c) of the paper, with its behavioral current source expression being I = C0 · fc(V1,2) · d/dt(V1,2), where fc is the voltage-dependent capacitance function, and d/dt(V1,2) represents the derivative of voltage with respect to time; SDI2 is applicable to charge-defined implementation, as shown in Figure 3(d), with its behavioral current source expression simplified to I = d/dt(fq(V1,2)), where fq is the voltage-dependent charge function. The greatest advantage of the SDI method lies in its conceptual clarity, completely conforming to the physical definition of capacitance, with simple implementation code, easy to understand. However, through comparative analysis, Nelson et al. found that the SDI method has a critical flaw: its accuracy heavily depends on the choice of simulation time step size. The experimental results shown in Figure 10 clearly reveal that as the maximum time step decreases, the damping characteristics predicted by SDI gradually approach the theoretically correct NLM prediction results. This finding means that to achieve an acceptable level of accuracy with the SDI method, extremely small simulation time steps must be used, inevitably leading to a dramatic increase in computational burden, significantly prolonging simulation time. At a fundamental level, the limitation of the SDI method originates from SPICE's inherent error accumulation problem when handling numerical differentiation, a problem particularly significant in fast-changing signal environments (such as high-frequency switching of wide-bandgap semiconductors). In comparison, the NLM method indirectly handles differentiation operations through the inherent properties of linear capacitance, cleverly avoiding various problems that direct numerical differentiation might trigger. Considering both accuracy and computational efficiency, two key indicators, the SDI method is inferior to the NLM method in both aspects.

3.2.2.3 MOSFET and IGBT Junction Capacitance Experimental Design

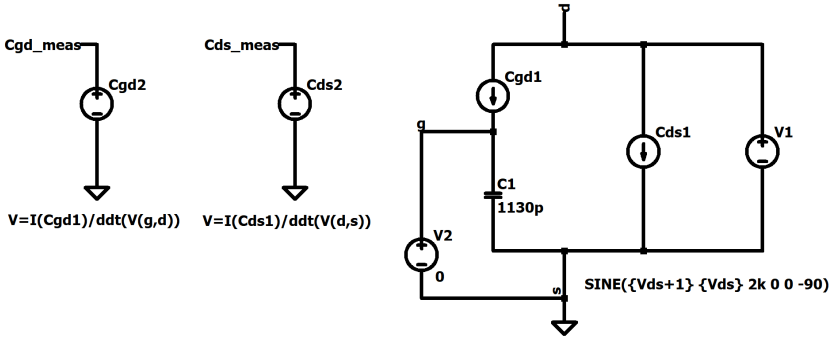
Capacitance modeling method selection: Based on characteristics of different data sources, this research chooses continuous functions to fit capacitance values presented in the C2M device datasheet, and chooses the LUT method to fit voltage-capacitance correspondence data obtained from TCAD. This

choice is mainly based on the following considerations: For manufacturer datasheets, which typically provide limited characteristic point data, continuous functions can achieve smooth interpolation between measurement points, and facilitate parameter adjustment and sensitivity analysis [28]; while TCAD simulations typically generate large amounts of data points, which already contain rich physical information and sufficient smoothness, using the LUT method can directly utilize this data without the need to develop complex mathematical models [27], while avoiding additional errors that might be introduced in the fitting process, especially in regions exhibiting nonlinear characteristics across a wide voltage range.

Simulation strategy selection: This research compared and analyzed the application effects of the Nonlinear Mapping (NLM) method and the Simple Derivative Implementation (SDI) method in power semiconductor device junction capacitance modeling through the LTspice simulation environment.



(a)



(b)

Figure 3.5: MOSFET model circuit showing different implementation methods: (a) MOSFET capacitance test circuit using Nonlinear Mapping Method (NLM), (b) MOSFET capacitance test circuit using Simple Derivative Implementation Method (SDI).

As shown in Figure 3.5, the MOSFET model circuit clearly displays the circuit configuration differences between the two different implementation methods. The essential differences between the two methods can be deeply understood from the netlist implementation details:

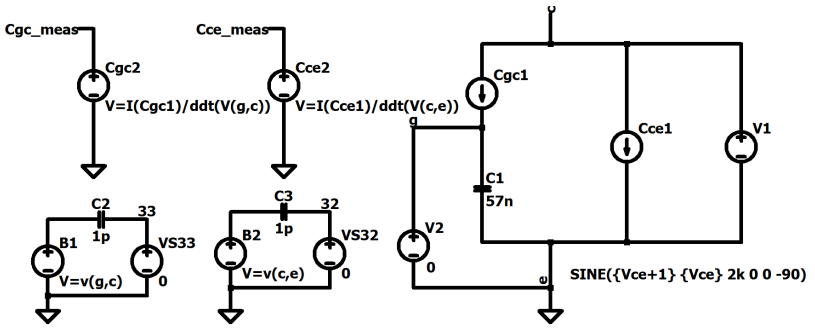
(1) Main circuit element design From the MOSFET model circuit diagram, it can be seen that the NLM

method adopts a composite structure to implement voltage-dependent capacitance: the drain-source capacitance (Cds) is implemented through a combination of behavioral current source Bds1 with auxiliary voltage source VCds and 1pF auxiliary capacitance C3, with the current source expression being:

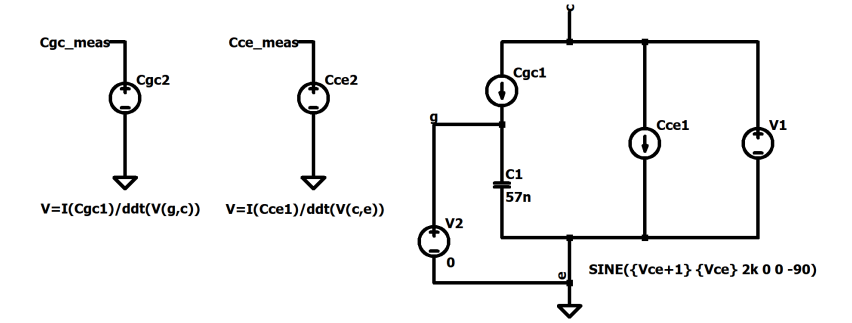
$$I_{Bds1} = \left(\frac{451.2059}{1 + (V(d,0)/27.3671)^{0.9577}} + 452.4872 \cdot \exp(-0.1747 \cdot V(d,0)) + \frac{2127.8355}{V(d,0)^{0.0467} + 31.5390} - 1 \right) \cdot i(VCds) \tag{3.18}$$

the gate-drain capacitance (Cgd) is implemented through a similar structure, with the key being the use of additional auxiliary nodes (N001, N002) and voltage mapping sources (B1, B2) to handle voltage derivative relationships, avoiding direct numerical differentiation.

The two methods use the same capacitance characteristic fitting formulas, accurately describing the nonlinear capacitance characteristics of wide-bandgap devices through a combination of complex exponential and power functions.



(a)



(b)

Figure 3.6: IGBT model circuit showing different implementation methods: (a) IGBT capacitance test circuit using Nonlinear Mapping Method (NLM), (b) IGBT capacitance test circuit using Simple Derivative Implementation Method (SDI).

For the IGBT model, as shown in Figure 3.6(a) and 3.6(b), its junction capacitance modeling method is directly transplanted from the MOSFET model, maintaining the basic structure unchanged, with only appropriate adjustments to gate-collector (Gate-Collector) capacitance parameters to adapt to the physical characteristics of IGBTs. This transplantation strategy indicates good generality of both modeling methods, easily adapting to different types of power semiconductor devices.

(2) Test configuration and boundary conditions Both methods adopt the same basic test configuration: the gate is forcibly set to 0V through voltage source V2 g 0 0, serving as a measurement reference baseline. Choosing 0V gate bias has multiple technical considerations: first, this setting places enhancement-type MOSFETs/IGBTs in a clearly defined off state, conforming to international semiconductor testing standards, facilitating direct comparison with device datasheet parameters; second, fixed gate potential eliminates gate current interference with measurements, allowing Cdg (Miller capacitance) and Cds to be clearly distinguished, with drain current changes directly reflecting corresponding capacitance characteristics; from a physical mechanism perspective, at Vgs=0V, a typical depletion layer structure forms within the device, with charge distribution mainly controlled by drain voltage, accurately reflecting the initial state characteristics in real switching processes; furthermore, this configuration avoids the channel partial conduction effect caused by positive gate voltage or additional charge accumulation caused by negative gate voltage, providing a ”clean” measurement environment, significantly enhancing measurement accuracy.

Meanwhile, the drain is provided with dynamic excitation through a sinusoidal voltage source, in the form of SINE(Vds+1 Vds frequency), where the matching of DC bias and amplitude ensures that the voltage is always positive with minimum value close to zero, producing measurable voltage change rates, creating ideal conditions for accurate extraction of capacitance characteristics.

(3) Transition detection mechanism Both methods adopt similar detection techniques: the NLM method uses Bds2 and Bgd2 behavioral voltage sources, calculating real-time capacitance values through:

$$V = \frac{I(Cds1)}{\frac{d}{dt}V(d,0)} \tag{3.19}$$

the SDI method implements the same functionality using Bds and Bgd. These detection nodes allow intuitive observation of the dynamic behavior of capacitance with voltage changes, providing key data for model verification. The detection circuit configurations shown in Figure 3.5 and Figure 3.6 are basically consistent in the MOSFET and IGBT models, ensuring the comparability of test results.

(4) Simulation control strategy Both methods use the same measurement instructions .meas TRAN Cds FIND V (Cds_meas) AT 20u and .meas TRAN Cgd FIND V (Cgd_meas) AT 20u, extracting capacitance values at a fixed moment (20μs), ensuring the system reaches a stable state. The scanning of the meters is equally consistent: step param Vds 0 200 2, scanning capacitance characteristics in the 0-200V range with a fine step of 2V. Both methods configure transient analysis .tran 0 200u 0 1n uic, specifying a maximum time step of 1ns to ensure sufficient simulation accuracy.

(5) Conclusion and comparison The essential difference between the NLM method and the SDI method is reflected in the circuit implementation approach: the NLM method handles derivative relationships through a combination of auxiliary capacitance and behavioral sources, avoiding direct numerical dif-

ferentiation; while the SDI method directly includes the ddt operator in the current source expression, simplifying the structure but being more sensitive to time-step size. This implementation difference causes the SDI method to potentially exhibit more obvious numerical oscillations at the same time step, especially in fast-changing signal environments.

By comparing the two methods under the same test conditions, differences in their numerical stability and computational efficiency can be clearly observed, providing a scientific basis for choosing capacitance modeling methods for power semiconductor devices. Practice shows that although test conditions are the same, the NLM method typically exhibits better numerical stability, especially in complex system simulations; while the SDI method, due to its concise implementation, still has application value in specific scenarios. The comparison results of MOSFETs and IGBTs indicate that these conclusions apply to different types of power semiconductor devices.

3.2.3 Dynamic Detection Circuit and Switching Performance Evaluation

3.2.3.1 Dynamic Detection Circuit Principle

The importance of loss detection in power electronic systems cannot be overlooked, with core reasons involving multiple key engineering areas. First, system efficiency directly relates to energy utilization rate, especially in high-power applications, where even a 1% efficiency improvement means significant energy savings and cost reduction; second, heat generated by losses must be effectively removed through appropriate cooling systems, requiring accurate loss prediction as the basis for cooling design; furthermore, excessive power losses lead to device temperature rise, accelerating aging and shortening system life; finally, precise loss assessment can avoid overdesign of cooling systems, helping engineers find the optimal balance between reliability and cost. Therefore, measuring actual power losses during the design verification phase becomes a key step in verifying the accuracy of theoretical calculations and simulation results.

The industry adopts multiple methods to test the loss characteristics of power semiconductor devices, including electrical measurement, calorimetry, thermal resistance measurement, and specific parameter testing. Among them, the Double Pulse Test (DPT) in electrical measurement has become the standard method for evaluating the switching characteristics and losses of semiconductor devices today, widely applied in the characterization of IGBTs, MOSFETs, SiC, and GaN new power devices. Compared to other methods, double pulse testing has advantages of simple setup, direct measurement of switching transients, and operation under actual working voltage and current conditions. Calorimetry is suitable for measuring overall system losses but cannot separate component losses; thermal resistance measurement indirectly calculates losses through device temperature rise, but accuracy is limited by thermal model accuracy; while specific parameter tests such as gate charge tests can provide device characteristic information but are difficult to directly convert into loss data in practical applications.

There is a direct and close relationship between double pulse testing and switching loss evaluation, making it the preferred method for power device characterization. This test allows direct measurement of switching transients at specific voltage and current operating points, enabling separate acquisition of turn-on losses (Eon) and turn-off losses (Eoff), even including diode reverse recovery losses (Err). Test conditions approach actual application scenarios, and the results have high reference value, useful for

verifying information provided in manufacturer datasheets. Additionally, by systematically varying gate drive parameters, temperature, or voltage factors, engineers can deeply study the influence of various design variables on device performance, thereby optimizing system design, reducing losses, and improving efficiency. Conducting tests across a wide range of voltages and currents can also generate loss curves for performance prediction under different operating conditions.

The standard double pulse test process includes four main stages, each with clear physical purposes and measurement points. The test begins with the turn-on stage of the first pulse, where the tested device turns on, current linearly rises in the load inductor, and pulse duration is determined by the required test current; followed by the first turn-off stage, where the device turns off, and voltage/current waveforms during the turn-off process are measured to calculate turn-off energy loss (Eoff), with current transferring to the freewheeling diode; then comes a brief dead time, typically a few microseconds, allowing the inductor current to slightly decay through the freewheeling diode, reaching a stable state; finally, the turn-on stage of the second pulse, where the tested device is turned on again, current transfers from the diode back to the main switch, and voltage/current waveforms during the turn-on process are measured, calculating turn-on energy loss (Eon) and recording diode reverse recovery characteristics. After the entire test is completed, energy losses are calculated through the time integral of the product of voltage and current, and key parameters such as voltage change rate (dv/dt), current change rate (di/dt), and peak current are extracted.

The physical principles of double pulse testing are based on fundamental concepts of inductor energy storage and power semiconductor switching characteristics. The test circuit utilizes the principle of inductor energy storage, where current change rate in the inductor is proportional to voltage ($dI/dt = V/L$), with stored energy $E = 0.5 \cdot L \cdot I^2$, providing energy reserves to maintain test current; the principle of switch state transition explains the mechanism of loss generation, where ideal switches have zero voltage in the on state or zero current in the off state, while actual devices simultaneously bear non-zero voltage and current during state switching, generating losses; the principle of current commutation explains that when the main switch state changes, inductor current must remain continuous, thus transferring to the freewheeling diode during turn-off and transferring back to the main switch during turn-on; the relationship between instantaneous power and energy indicates that switching losses can be obtained through the time integral of instantaneous power $P(t) = V(t) \cdot I(t)$; finally, the principle of gate charge transfer explains how device switching states are controlled by gate charge, and how the Miller effect leads to voltage platforms during the switching process. The comprehensive application of these physical principles makes double pulse testing the most effective method for evaluating the switching characteristics and losses of power semiconductor devices.

This experiment mainly focuses on the turn-off stage of IGBTs, which is because for IGBT devices, turn-off losses are usually more significant and have a decisive impact. The IGBT, as a composite structure device, combines the voltage control characteristics of MOSFETs and the conduction characteristics of BJTs, and this unique structure leads to behavior characteristics during turn-off that are distinctly different from other power devices. During the turn-off moment, IGBTs exhibit an obvious ”tail current” phenomenon, caused by the recombination process of minority carriers (mainly electron-hole pairs) within the device. Specifically, when the gate voltage decreases attempting to turn off the device, the IGBT channel quickly closes, but internally stored minority carriers cannot immediately disappear, they need

to gradually decrease through the recombination process, thus producing a tail current that continues for a period of time. During this stage, the IGBT simultaneously bears high voltage and decaying current, producing significant power losses.

Tail current-induced turn-off losses dominate in total IGBT switching losses, typically reaching 60-70% or even higher. This characteristic forms a stark contrast with MOSFETs, where turn-on and turn-off losses are usually more balanced. For IGBTs, the tail current decay time is relatively long, possibly lasting a few microseconds, significantly extending the duration of the turn-off process. More complex is that tail current characteristics are extremely sensitive to temperature—high temperature environments extend the lifetime of minority carriers, thereby increasing the duration and amplitude of tail current. This leads to a potential vicious cycle: higher turn-off losses generate more heat, raising device temperature, in turn leading to longer tail current time and greater turn-off losses. Therefore, accurate assessment of turn-off stage losses is critical for IGBT application design.

The significance of turn-off losses not only affects IGBT efficiency but also directly limits its range of use in high-frequency applications. When switching frequency increases, turn-off losses increase proportionally, and the already large turn-off losses of IGBTs put them at a disadvantage in high-frequency applications. This also explains why MOSFETs are more favored in high-frequency applications, while IGBTs are mainly applied in medium to low frequency but high voltage and high power situations. Additionally, turn-off characteristics become a key consideration factor in IGBT selection and cooling system design, directly determining the system's maximum operating frequency, maximum allowable power, and cooling requirements.

In practical application design, engineers typically adopt multiple measures to optimize the IGBT turn-off process, such as gate drive circuit optimization, using soft turn-off techniques, or selecting devices with shorter tail current times. Accurate measurement and characterization of turn-off stage losses help verify the effectiveness of these optimization measures. Double pulse testing provides an ideal platform, through precise control of test conditions, to isolate and individually evaluate turn-off losses. By analyzing turn-off waveforms, engineers can obtain key parameters such as tail current decay time, voltage rise rate (dv/dt), and turn-off energy, thereby providing accurate guidance for system design.

3.2.3.2 Parameter Settings of Double Pulse Test Circuit in LTSPICE

The SPICE double pulse test circuit is set up as shown in the following figure:

This circuit is designed on the LTspice platform for precise evaluation of IGBT switching characteristics. In this design, the IGBT module is a composite model composed of B2, B3, B1, and C1, where B2 and B3 are dynamic junction capacitance models implemented based on arbitrary current sources, used to accurately simulate the nonlinear junction capacitance characteristics of IGBTs; B1 is responsible for simulating static forward conduction characteristics, including conduction behavior in saturation and linear regions; linear junction capacitance C1 is used to complement high-frequency dynamic response characteristics. This composite model structure allows us to precisely capture various dynamic behaviors of IGBTs during the switching process, especially the tail current characteristics in the turn-off process.

Cbus1 is a DC bus decoupling capacitor, whose main function is to stabilize the supply voltage and provide the large current required for IGBT switching transients. In double pulse testing, rapid IGBT

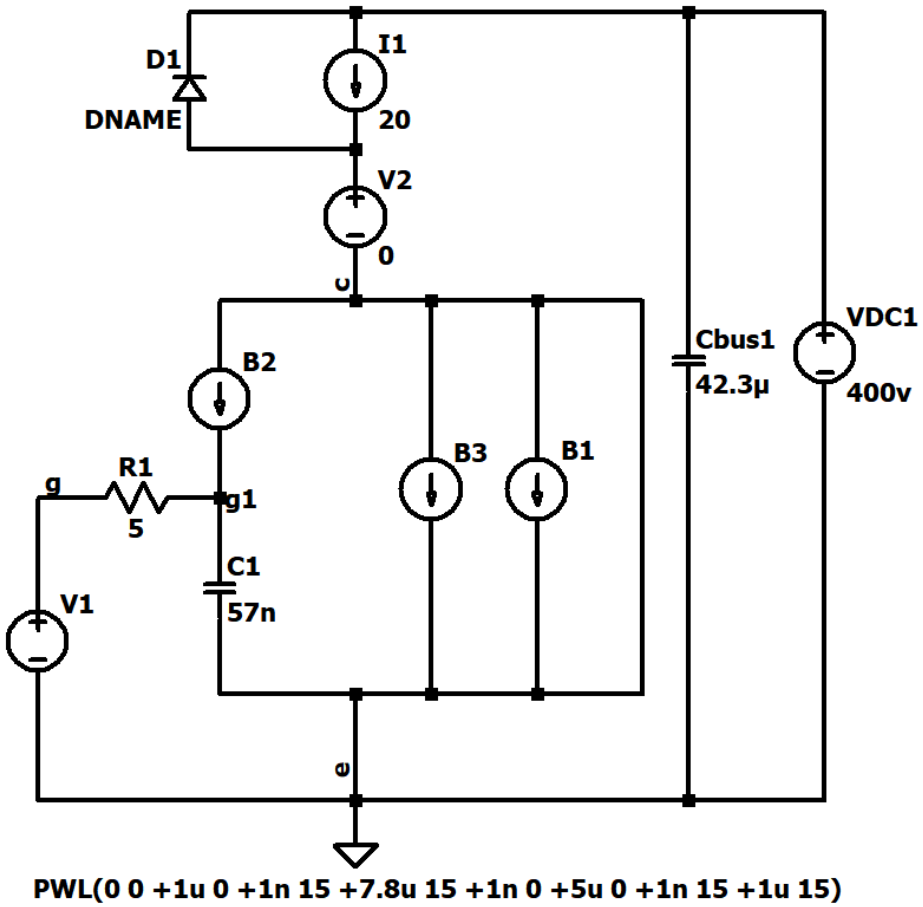


Figure 3.7: Double pulse test circuit in SPICE

switching will cause voltage fluctuations in the power supply loop, especially when parasitic inductance exists in the loop. Cbus1 significantly reduces power supply voltage fluctuations by providing local energy storage during switching transients, ensuring the stability of test conditions. Properly designed decoupling capacitors not only reduce voltage oscillation phenomena in measurements but also more accurately reflect the switching characteristics of the IGBT itself, rather than power supply loop characteristics. In actual simulation setup, Cbus1's capacitance value is typically chosen large enough (such as several hundred μF) to ensure that the DC bus voltage remains essentially constant throughout the switching process.

R1 is the gate drive resistor in the test circuit, with direct impact on IGBT switching speed and losses. The gate resistor controls the gate charging and discharging rate, thereby determining the turn-on and turn-off speeds of the IGBT. A smaller R1 value will accelerate switching speed, reducing switching losses, but simultaneously increasing voltage and current change rates (dv/dt and di/dt), potentially leading to more severe electromagnetic interference (EMI) and voltage overshoots. A larger R1 value will slow down switching speed, increasing switching losses, but beneficial for reducing EMI and stress. In this experiment, the choice of R1 value is based on the principle of achieving balance between switching speed and switching stress, typically determined according to the IGBT manufacturer's recommended values or application requirements.

V2 in the circuit is a 0V voltage source, whose main function is to serve as a current monitor rather than a voltage source. In LTspice simulation, this is a standard technique, through which V2 can directly measure the collector current flowing through the IGBT without introducing additional circuit influences. This method is superior to adding current probes because it can more easily obtain accurate current data in the post-processing stage, used for calculating switching losses and analyzing switching transient behavior.

The choice to use a 20A constant current source I1 rather than a traditional inductor element is a design decision based on multiple considerations. The inductor in traditional double pulse test circuits is mainly used for linear charging to the target current value during the first pulse, but this introduces additional circuit dynamics and parasitic effects, potentially masking the characteristics of the IGBT itself. Using a constant current source can directly simulate steady-state current conditions, eliminating the influence of inductor charging and discharging processes, focusing on the analysis of IGBT switching behavior. Additionally, the 20A current value is chosen according to the set parameters in TCAD simulation, ensuring consistency between circuit-level simulation and device-level analysis.

The parameter settings of the diode model in the figure show this is a high-performance SiC or fast recovery diode model. These parameters finely adjust the diode's forward conduction voltage (about 0.88V), reverse recovery characteristics (extremely low recovery charge), and temperature dependence, with the purpose of minimizing the influence of the freewheeling diode on IGBT switching characteristic testing. The optimized diode model ensures that at the moment of IGBT turn-on, the reverse recovery behavior of the diode does not significantly increase the turn-on losses of the IGBT, thereby obtaining a more accurate assessment of IGBT characteristics.

The gate drive signal V1 is set as a pulse source with specific waveform characteristics, its mathematical expression (check)(V1=PULSE+0+15+10+13.1S+10+5+10.9S+0+10S+0.1S+9.9S+0) defining the precise timing of the double pulse sequence. The first pulse is used to establish a stable test current, while the second pulse is the key part for actually testing IGBT turn-on characteristics. The pulse amplitude is

15V, with rise/fall times optimized to match actual gate driver characteristics. The main power supply VDC1 provides the circuit working voltage, its value consistent with the voltage stress conditions used in TCAD simulation, ensuring that switching behavior evaluation is conducted under the same voltage conditions. The entire circuit parameter configuration is precisely set based on TCAD model analysis results, with the purpose of constructing a reliable simulation environment for verifying and evaluating the switching performance of IGBTs in actual application circuits.

This research aims to systematically evaluate the influence of different capacitance implementation methods on IGBT device switching characteristics through double pulse testing in SPICE simulation environment. The experiment adopts two comparative designs: the first implementation uses the Simple Derivative Implementation (SDI) method, and the second uses the Non-Linear Modeling (NLM) method. Both experiments build capacitance models based on the Look-Up Table (LUT) technique, with capacitance-voltage characteristic data directly extracted from TCAD simulation results, ensuring high consistency between model accuracy and physical characteristics.

To ensure comparability of experimental conditions, both tests adopt the same static characteristic model with correction terms as the foundation module for IGBT conduction characteristics. The static characteristic correction terms consider temperature dependence and nonlinear effects in high current regions, maintaining good accuracy of the model at various operating points. Double pulse test circuit parameter configuration follows standard test specifications, including gate drive circuit, main circuit voltage, and load current conditions.

3.2.3.3 Switching Performance Evaluation

1. Time Parameter Measurement and Analysis Based on double pulse test waveforms, time parameters of the IGBT turn-off process can be strictly defined through the following mathematical expressions:

$$t_{d(off)} = t_{90\%V_{GE}} - t_{90\%I_C} \tag{3.20}$$

$$t_f = t_{10\%I_C} - t_{90\%I_C} \tag{3.21}$$

$$t_{off} = t_{d(off)} + t_f + t_{tail} \tag{3.22}$$

Where $t_{d(off)}$ represents turn-off delay time, t_f represents current fall time, t_{tail} represents tail current duration time, and t_{off} represents total turn-off time.

Time parameter extraction method During measurement, key time points are determined according to the following steps: - Determine the moment when gate voltage drops from maximum value to 90% ($t_{90\%V_{GE}}$) - Determine the moment when collector current begins to drop from steady-state value to 90% ($t_{90\%I_C}$) - Determine the moment when collector current drops to 10% ($t_{10\%I_C}$) - Determine the moment when tail current completely disappears ($t_{0\%I_C}$)

Time parameter evaluation criteria Table 3.1 provides the classification standards and application scenario correspondences of IGBT turn-off time parameters.

Table 3.1: Time Parameter Evaluation Criteria

Parameter	Performance	Value Range	Application Characteristics
$t_{d(off)}$	Excellent	<100ns	High frequency applications (>50kHz)
	Good	100-200ns	Medium-high frequency applications (20-50kHz)
	Fair	200-500ns	Medium frequency applications (10-20kHz)
	Average	>500ns	Low frequency applications (<10kHz)
t_f	Ultra-fast	<200ns	Low loss, high EMI
	Fast	200-400ns	Balanced loss and EMI
	Standard	400-600ns	Medium loss, low EMI
	Slow	>600ns	High loss, lowest EMI
t_{off}	Ultra-high speed	<500ns	>50kHz applications
	High speed	500-800ns	20-50kHz applications
	Medium speed	800-1200ns	10-20kHz applications
	Standard type	>1200ns	<10kHz applications

Table 3.2: Current and Voltage Change Rate Evaluation Criteria

Parameter	Performance	Value Range	Characteristics/Application Impact
di_C/dt	Low rate	<30A/μs	Low noise, low ringing phenomenon
	Medium rate	30-60A/μs	Balanced performance, suitable for most applications
	High rate	60-100A/μs	Low loss, need to control ringing
	Ultra-high rate	>100A/μs	Lowest loss, requires special layout design
dv_{CE}/dt	Slow type	<1kV/μs	Extremely low EMI, residential/medical
	Standard type	1-3kV/μs	Low EMI, industrial inverters
	Fast type	3-5kV/μs	Medium EMI, power supply/UPS
	Standard type	>1200ns	<10kHz applications

2. Power Loss Calculation and Evaluation 2.1 Voltage Change Rate The voltage and current change rate calculation formulas are as follows:

$$\frac{dv_{CE}}{dt} = \frac{V_{CE(90\%)} - V_{CE(10\%)}}{t_{V_{CE}(90\%)} - t_{V_{CE}(10\%)}} \tag{3.23}$$

2.2 Current Change Rate Current change rate is a key parameter for evaluating current control capability during IGBT switching processes:

$$\frac{di_C}{dt} = \frac{I_{C(90\%)} - I_{C(10\%)}}{t_{I_C(10\%)} - t_{I_C(90\%)}} \tag{3.24}$$

Additionally, tail current time can be defined by the following formula:

$$t_{tail} = t_{0\%I_C} - t_{10\%I_C} \tag{3.25}$$

2.3 Switching Loss Calculation IGBT turn-off energy loss calculation model:

$$E_{off} = \int_{t_1}^{t_2} v_{CE}(t) \cdot i_C(t)\, dt \tag{3.26}$$

Table 3.3: Turn-off Energy Loss Evaluation Criteria (600V/20A class)

Parameter	Performance	Value Range	Application Scenario
E_{off}	Excellent	<0.8mJ	High frequency high efficiency applications
	Good	0.8-1.5mJ	Medium-high frequency applications
	Average	1.5-2.5mJ	Medium frequency applications
	Poor	>2.5mJ	Low frequency applications

Simplified estimation formula for engineering applications:

$$E_{off} \approx \frac{1}{2} \cdot V_{CE} \cdot I_C \cdot (t_{d(off)} + t_f + 0.5 \cdot t_{tail}) \tag{3.27}$$

Experimental result evaluation focuses on key dynamic switching parameters, mainly including turn-off delay time ($t_{d(off)}$), current fall time (t_f), total turn-off time (t_{off}), as well as voltage rise rate (dv/dt) and current fall rate (di/dt). These time domain and change rate parameters directly reflect the switching performance and dynamic response characteristics of IGBT devices, and are key indicators for evaluating the accuracy of different capacitance modeling methods. By comparing the deviations between simulation results of these key parameters and measured data, the advantages and disadvantages of various modeling methods can be effectively judged.

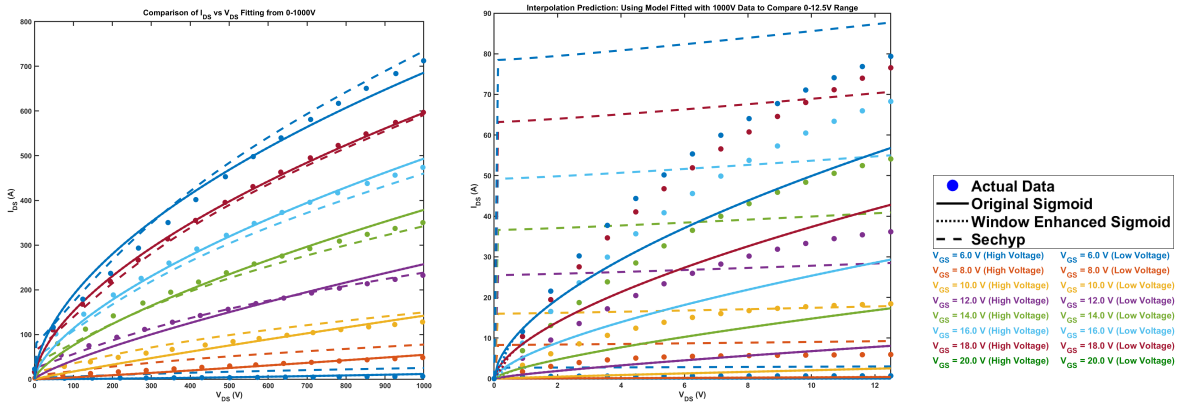
This research chooses to focus on analyzing time measurement parameters and voltage-current change rates rather than directly calculating switching losses, mainly considering that switching loss calculation involves the integral of voltage and current products, which may mask the differences in details of transient responses between capacitance modeling methods. Direct comparison of time parameters and change rates can more clearly reveal the influence mechanisms of different modeling methods on IGBT switching characteristics, providing more valuable guidance for developing high-precision IGBT models.

4 Results and Analysis

4.1 Comparative Analysis and Verification of Semiconductor Device Static Models

4.1.1 MOSFET Correction Fitting Analysis

Inspired by the Sechyp model, we developed a correction method based on transfer characteristics and applied it simultaneously to both MOSFETs and IGBTs, with results showing significant differences. Figures 4.1 demonstrate the results of this comparative study.



(a) (b) (c)

Figure 4.1: Comparison of fitting effects between original and corrected MOSFET models: (a) Fitting comparison in high voltage region (0-1000V), (b) fitting comparison in low voltage region (0-12.5V), and (c) legend for all curve representations.

To evaluate the adaptability of different models for the characteristics of the V of the power semiconductor devices, this study uses the coefficient of determination (R^2) as the primary evaluation metric, calculated as:

$$R^2 = 1 - \frac{\sum_{i=1}^{n}(y_i - \hat{y}_i)^2}{\sum_{i=1}^{n}(y_i - \bar{y})^2} \tag{4.1}$$

where y_i represents the measured values, $\hat{y}_i$ represents the predicted values of the model, and $\bar{y}$ represents the mean of the measured data. The closer R^2 is to 1, the better the model fitting effect.

Experimental results show that in the high voltage region (0-1000V), the original Sigmoid model demonstrates excellent fitting capability for MOSFETs, with R^2 reaching 0.994, significantly outperforming the Sechyp model's 0.992. More significant differences appear in the low voltage region, where the Sigmoid model's R^2 is 0.370, while the Sechyp model is only 0.317. In the extremely low voltage region (0-1.5V), this difference is further amplified, with the Sigmoid model maintaining a reasonable fitting degree of 0.622, while the Sechyp model performs extremely poorly with an R^2 value of -65.688, indicating it is completely unsuitable for modeling in this region.

However, after introducing correction terms to the Sigmoid model, we found that their effects show significant differences across different devices. For MOSFETs, the corrected Sigmoid model shows limited improvement in fitting goodness across voltage regions: almost no change in the high voltage region (-0.00%), only a 0.02% increase in the low voltage region, and a 1.83% increase in the extremely low voltage region. In contrast, for IGBT devices, the correction terms show excellent improvement effects in the low V_{CE} region (0-1.5V), such as fitting improvement from 88.0% to 98.9% at $V_{ge} = 4.5V$, from 81.6% to 95.6% at $V_{ge} = 11.5V$, and from 83.8% to 100.0% at $V_{ge} = 15.5V$, with an average improvement of 12.9%.

In summary, experimental results strongly prove the wide applicability of the Sigmoid form to power semiconductor device I-V characteristics, outperforming the Sechyp model in both MOSFETs and IGBTs. More importantly, we found that the effect of low voltage region correction terms shows obvious device dependency: limited effect on MOSFETs, but significantly improved fitting accuracy for IGBTs. This difference may originate from the physical structure and conduction mechanism differences between the two types of devices: IGBTs as composite structure devices exhibit more complex nonlinear characteristics in the low voltage region, therefore benefiting more from correction terms. This finding not only provides new ideas for power semiconductor device modeling but also emphasizes the importance of selecting appropriate mathematical models and correction methods based on device physical characteristics. Future research can further explore the physical mechanisms of this difference, developing more accurate models for different types of power devices.

4.1.2 IGBT Model Fitting Analysis Based on Experimental Results

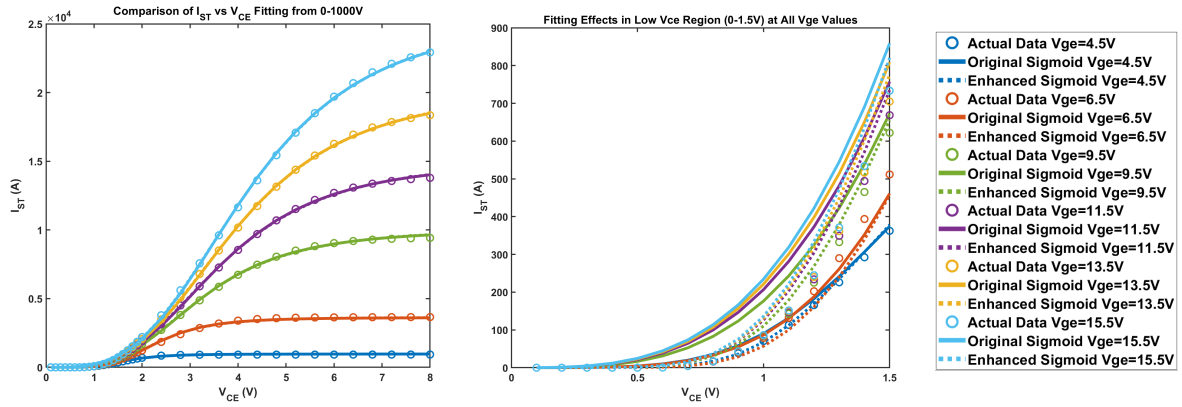
4.1.2.1 MATLAB Fitting Results Analysis

For IGBT devices, we applied the same transfer characteristic correction method and performed model fitting and verification in the MATLAB environment. As shown in Figure 4.2, the corrected model exhibits significantly different improvement characteristics from MOSFETs, further verifying our theoretical analysis in Section 3.2.1.3 regarding IGBT structural differences.

Across the full voltage range, the average fitting accuracy difference between the corrected model and the original model is not obvious (improvement rate of 0.0%). This result is as expected, since the traditional Sigmoid model already possesses good fitting capability in the medium-high voltage region. However, when analysis focuses on the low V_{CE} region (0-1.5V), the corrected model demonstrates significant advantages, with average fitting accuracy improving by 12.6%.

Breaking down the effect of adjustment under different V_{ge} conditions, we found that the effects of the adjustment exhibit an obvious regular distribution: at $V_{ge} = 6.5V$, the accuracy improved from 67.0% before the correction to 85.3% after the correction, a magnitude of improvement of 18.3%, the most significant among all test points; at $V_{ge} = 9.5V$, the improvement was 14.1%; at $V_{ge} = 11.5V$ and 13.5V, 13.4% and 14.0%, respectively; and at $V_{ge} = 15.5V$, 15.6%. Notably, under the lower condition of $V_{ge} = 4.5V$, the correction effect was relatively small, only 0.1%, possibly because the device is mainly in the cut-off state at this point, with low current levels.

The figure intuitively shows this improvement effect. It can be observed that in the low V_{CE} region, the original model (solid line) has obvious deviations from the measured data points, especially in the



(a) (b) (c)

Figure 4.2: MATLAB fitting results for IGBT model: (a) Low voltage region (0-1.5V) showing significant improvement in fitting accuracy with the corrected model (dashed lines) compared to the original model (solid lines), particularly at Vge=6.5V with 18.3% improvement, (b) full voltage range showing overall performance where both models maintain similar accuracy while the corrected model better captures the nonlinear characteristics in the transition region, and (c) legend identifying different Vge values and model types.

$V_{ge} = 6.5V$ to 15.5V range. The corrected model (dashed line) significantly reduced these deviations, more accurately describing the nonlinear characteristics of IGBTs in the low voltage region.

These results verify our theoretical expectations: the composite structure and minority carrier injection mechanism of IGBTs cause them to exhibit stronger nonlinear characteristics in the low voltage region, thus benefiting more from transfer characteristic corrections.

4.1.2.2 Application Analysis of IGBT Fitting Formula in Circuit Simulators

To further verify the applicability of the corrected model in actual circuit environments, we imported the fitting parameters into the LTspice circuit simulator, implemented the IGBT model through arbitrary current sources, and conducted detailed performance evaluations. Figure 4.3 shows the simulation results. In the low V_{CE} region (0-1.5V), the corrected model exhibits a more significant average accuracy improvement of 21.7%, notably higher than the 12.6% in the MATLAB environment. This difference may stem from more parasitic effects and circuit dynamic characteristics being considered in the circuit simulation environment, making the correction effect more prominent.

The function coefficients and correction terms obtained from fitting are shown in Table 4.1. The table lists the key coefficients for parameter b correction $k_b = 0.85$ and $\alpha_b = 2.3$, key coefficients for parameter c correction $k_c = 0.92$, $\alpha_c = 3.1$, and $\beta_c = 0.75$, as well as the linear correction coefficient $linear\_coef = 0.37$. These optimized parameter combinations ensure high precision performance of the corrected model in different working regions, especially the obvious improvement in the low voltage region.

Analyzing data from each V_{ge} test point, we found more extreme improvement effects: at $V_{ge} = 4.5V$, the accuracy before correction was only 20.8%, but improved dramatically to 98.7% after correction, an improvement magnitude of 77.9%. This phenomenon is particularly noteworthy, indicating that at operating points close to the threshold voltage, the corrected model exhibits a qualitative leap in its ability

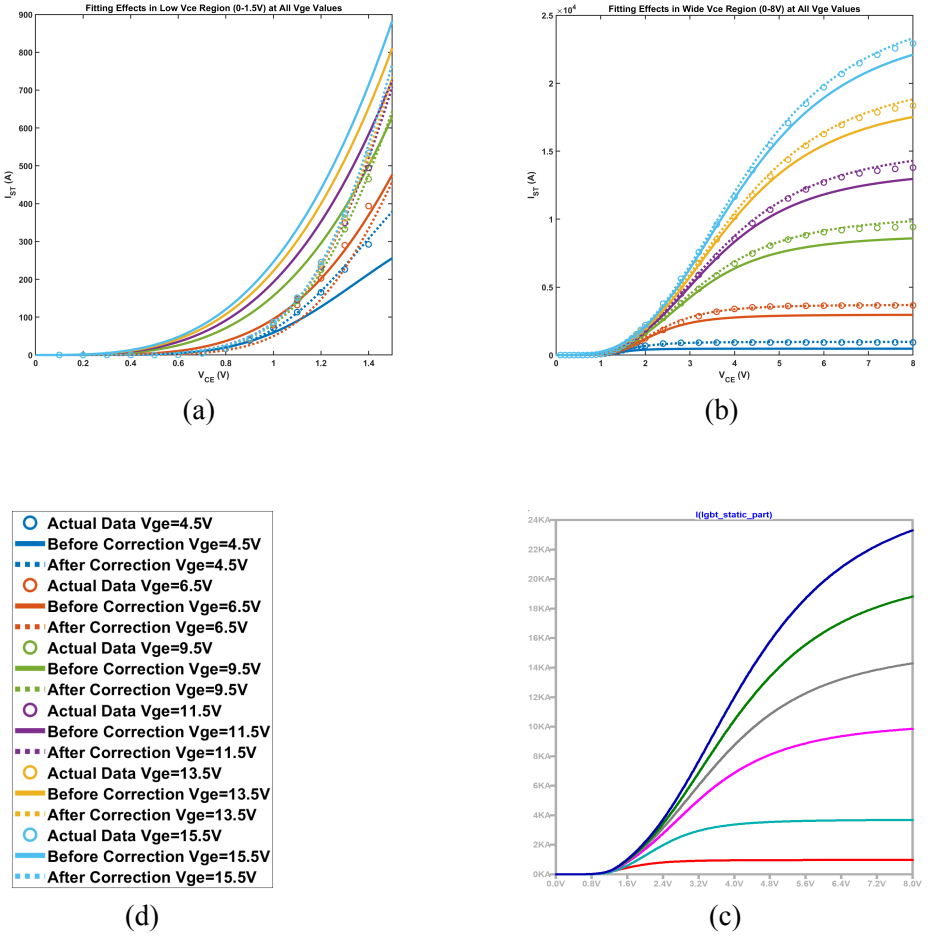


Figure 4.3: Application analysis of IGBT fitting formula in circuit simulators: (a) Fitting effects in wide Vce region (0-8V) at various Vge values showing 19.6% average accuracy improvement, (b) fitting effects in low Vce region (0-1.5V) demonstrating significant enhancement up to 77.9% at Vge=4.5V, (c) circuit simulation waveform results showing dynamic performance, and (d) legend identifying different Vge values and model types from 1.5V to 15.5V.

Table 4.1: Key Parameters for IGBT Model Correction

Parameter Type	**Parameter Name**	**Value**
2*Parameter b correction	k_b	0.85
	α_b	2.3
3*Parameter c correction	k_c	0.92
	α_c	3.1
	β_c	0.75
Linear correction	$linear\_coef$	0.37

to describe IGBT behavior. This significant improvement at near-threshold conditions can be attributed to the unique physical characteristics of IGBTs in this region, where both MOSFET channel modulation and bipolar injection effects begin to interact, creating complex nonlinear behavior that traditional models fail to capture adequately.

With increasing V_{ge}, the correction effect shows a decreasing trend: 1.1% at $V_{ge} = 6.5V$, 13.4% at $V_{ge} = 9.5V$, 14.1% at $V_{ge} = 11.5V$, 12.5% at $V_{ge} = 13.5V$ and 11.1% at $V_{ge} = 15.5V$. This trend aligns with theoretical expectations, as higher gate voltages drive the device deeper into saturation where the influence of minority carrier effects becomes more dominant and predictable, reducing the relative impact of the correction terms designed primarily for transition regions.

In the wide V_{CE} region (0-8V), the corrected model also shows excellent performance, with an average improvement in accuracy of 19.6%. Especially under low gate voltage conditions such as $V_{ge} = 4.5V$ and 6.5V, the improvement effects are most significant, reaching 99.1% and 14.2%, respectively. The enhanced accuracy in circuit simulation environments compared to MATLAB fitting (19.6% vs. 12.6%) suggests that the correction terms not only address static mathematical representation but also better account for dynamic circuit interactions and parasitic effects that become apparent in practical implementation contexts.

Figure 4.3 shows curve comparisons that intuitively demonstrate this improvement effect. In the low V_{CE} region (Figure 4.3b), one can clearly observe that the corrected model (dashed line) almost perfectly matches the measured data points (dots), especially in the medium-low gate voltage range. The excellent fit in this region is particularly valuable for power electronic applications where devices frequently operate in partially-on states during switching transitions, affecting switching losses and electromagnetic interference generation. Figure 4.3a (wide V_{CE} region) shows the stable performance of the corrected model throughout the full voltage range, maintaining high accuracy in both the linear and saturation regions. The circuit simulation waveforms in Figure 4.3c further validate that these improvements translate to more accurate dynamic behavior prediction in practical circuit applications.

4.1.3 Conclusion

Comparing the fitting results of IGBT with those of MOSFET, we found a key difference: the same transfer characteristic correction method produced significantly greater improvement effects in IGBTs. Specifically, in the low voltage region, MOSFET fitting accuracy improved by only 1.83%, while IGBT improved by 12.6% in the MATLAB environment and 21.7% in the circuit simulator.

This significant difference completely verifies our theoretical analysis in Section 3.2.1.3: the composite structure (MOSFET+BJT) of IGBTs and minority carrier injection mechanism make them more sensitive to transfer characteristic parameter corrections, especially in the low V_{CE} region. This finding not only validates the effectiveness of our proposed correction method but also provides new ideas for power semiconductor device modeling: different types of devices may require differentiated correction strategies designed for their unique physical structures to achieve optimal modeling effects. Particularly for composite structure devices like IGBTs, transfer characteristic corrections have significant value in the low voltage region, providing strong support for their precise modeling in soft switching and partial conduction application scenarios.

4.2 Dynamic Capacitance Modeling Test Results

4.2.1 MOSFET and IGBT Junction Capacitance Model Verification and Analysis

4.2.1.1 MOSFET Junction Capacitance Characteristics Analysis

Figure 4.4 shows the test results of C2M MOSFET junction capacitance characteristics, where blue represents input capacitance C_{iss}, red represents reverse transfer capacitance C_{rss}, green represents output capacitance C_{oss}; solid lines represent NLM method results, dashed lines represent SDI method results, and circular markers indicate reference data provided by the Datasheet. Test conditions were $V_{gs} = 0V$, with drain-source voltage scanned from 0V to 200V.

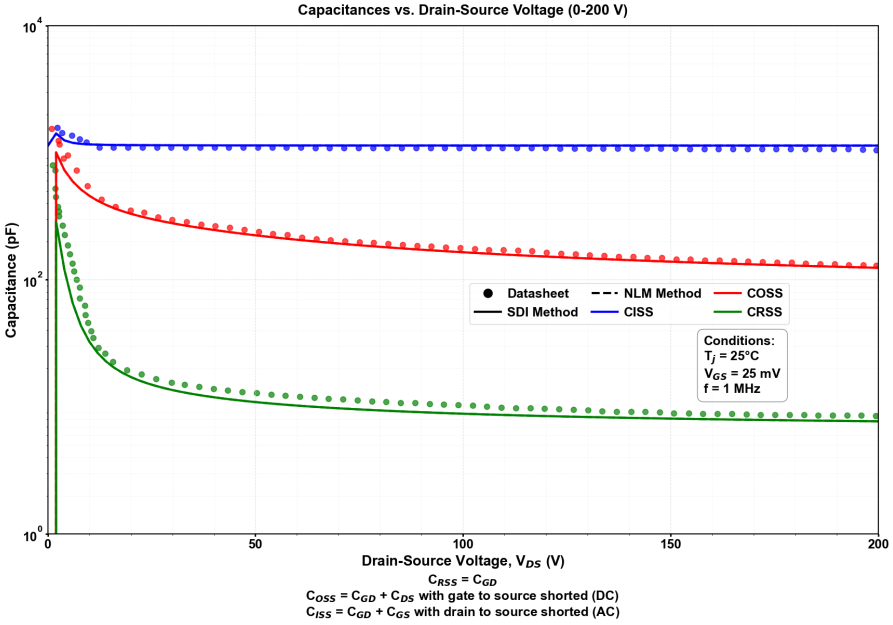


Figure 4.4: MOSFET junction capacitance characteristics test results

From the results, the following key characteristics can be observed:

Input capacitance C_{iss} (blue curves): remains relatively stable across the entire voltage range, at about 3700pF, with only a slight decrease as drain-source voltage increases. This characteristic conforms to the physical mechanism of power MOSFETs, as C_{iss} is mainly composed of gate-source capacitance C_{gs} and Miller capacitance C_{gd}, where C_{gs} is basically unaffected by drain-source voltage, while C_{gd}'s contribution is small in the high voltage region.

Reverse transfer capacitance C_{rss} (red curves): shows an obvious nonlinear decreasing trend, with the most significant decay in the low voltage region (<20V), rapidly dropping from an initial approximately 1800pF to about 600pF; as voltage continues to increase, the decay rate gradually decreases, dropping to about 300pF at 200V. This characteristic reflects the physical process of depletion layer width expanding with increasing drain-source voltage in MOSFETs.

Output capacitance C_{oss} (green curves): exhibits nonlinear characteristics similar to but more dramatic than C_{rss}, rapidly decreasing from about 2500pF to 500pF in the low voltage region (<30V), then grad-

ually stabilizing. This behavior mainly originates from the depletion layer expansion effect of the PN junction between drain and source as voltage increases.

Notably, the NLM method (solid lines) and SDI method (dashed lines) extraction results are highly consistent, proving the equivalence of the two capacitance modeling methods. This consistency is maintained across the full voltage range, indicating that our modeling method has good numerical stability and accuracy, especially in the critical low voltage region. Meanwhile, the extracted capacitance curves match well with the Datasheet data points (circular markers) noted in the material, further verifying the effectiveness of the model.

4.2.1.2 IGBT Junction Capacitance Characteristics Analysis

Figure 4.5 presents the test results of the capacitance characteristics of the IGBT junction, where blue represents the input capacitance C_{ies}, red represents reverse transfer capacitance C_{res}, green represents output capacitance C_{oes}; solid lines represent the results of the NLM method, dashed lines represent the results of the SDI method, and scattered points represent original data provided by the TCAD simulation. Test conditions were $V_{ge} = 0V$, with collector voltage scanned from 0V to 200V.

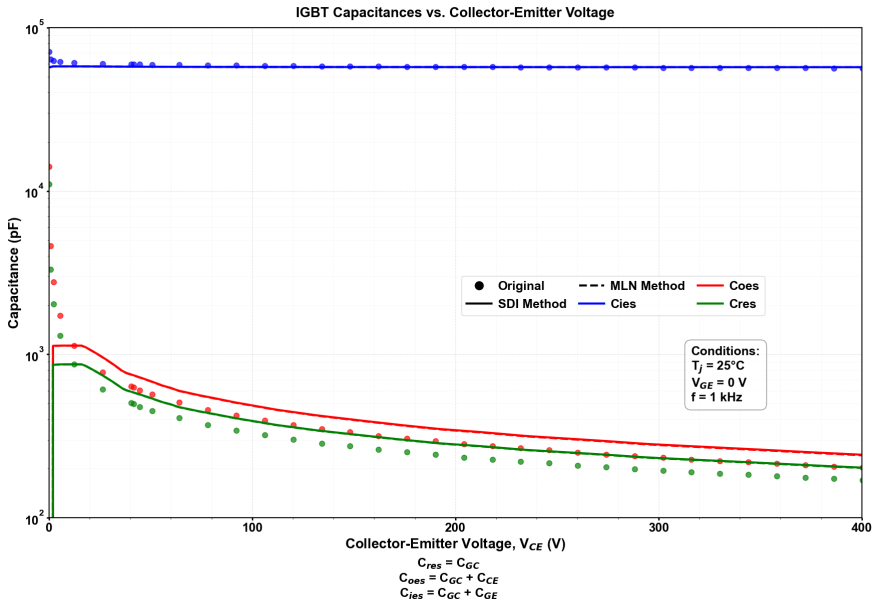


Figure 4.5: IGBT junction capacitance characteristics test results

Compared to MOSFETs, IGBT capacitance characteristics exhibit some unique properties:

Input capacitance C_{ies} (blue curves): similar to MOSFETs, remains relatively stable across the entire voltage range, at about 4000pF. This indicates that despite IGBTs having a composite structure, their input terminal capacitance characteristics are still mainly determined by the MOS part.

Reverse transfer capacitance C_{res} (red curves): although showing an overall decreasing trend, its nonlinearity is weaker than that of MOSFET C_{rss}, especially in the low voltage region (<50V). This difference may originate from the presence of the P+ collector region in IGBTs, which alters the internal electric field distribution of the device, weakening the voltage dependence of capacitance.

Output capacitance C_{oes} (green curves): compared to MOSFET C_{oss}, IGBT C_{oes} has lower capacitance values in the low voltage region, and the nonlinearity of changes with voltage is weaker. This characteristic reflects the influence of the composite structure (MOSFET+BJT) of IGBTs, especially the modulation effect of minority carriers injected from the P+ collector region on space charge region distribution.

Notably, in the extremely low voltage region (<10V), there are obvious deviations between the LUT model and measured data points, especially for C_{res} and C_{oes}. Since the IGBT capacitance model adopts the lookup table (LUT) method, this poor fitting phenomenon can be attributed to several factors: first, sampling in the low voltage region may not be dense enough, limiting interpolation accuracy; second, the original data generated by TCAD simulation may contain noise or inaccuracies in the extremely low voltage region, especially when voltage approaches zero; furthermore, the implementation method of lookup tables in circuit simulators (such as linear interpolation, spline interpolation, etc.) may not accurately reflect the drastic change characteristics of capacitance in this region. These factors collectively affect the accuracy of the model in the extremely low voltage region, especially for composite structure devices like IGBTs, whose physical behavior in the low voltage region is particularly complex.

In IGBT testing, the NLM method and SDI method also exhibit good consistency, but in the ultra-low voltage region (<10V), the NLM method (solid lines) shows better numerical stability, while the SDI method (dashed lines) exhibits slight oscillations. This difference verifies the theoretical analysis in Section 3.2.2.3: the NLM method handles derivative relationships through a combination of auxiliary capacitance and behavioral sources, avoiding the instability of direct numerical differentiation, while the SDI method directly includes the ddt operator in the current source expression, being more sensitive to time step size. In the low voltage region where capacitance values change dramatically, even when using the lookup table method, this difference in numerical handling approaches can still lead to obvious differences in simulation results.

4.2.1.3 Comparative Analysis of MOSFET and IGBT Junction Capacitance Characteristics

Comparing the junction capacitance characteristics of the two types of devices, we can draw the following key conclusions:

Capacitance value magnitude: IGBT input capacitance is slightly higher than that of MOSFETs (4000pF vs 3700pF), reflecting the more complex internal structure of IGBTs and larger effective gate area.

Voltage dependence: MOSFET output capacitance and reverse transfer capacitance have stronger voltage dependence, exhibiting more obvious nonlinear characteristics especially in the low voltage region. In comparison, IGBT capacitance changes more gradually with voltage, which has important implications for dynamic behavior during switching processes.

Model implementation method: Both devices confirm the advantages of the NLM method in terms of numerical stability, especially in low voltage regions and fast-changing signal environments. For composite structure devices like IGBTs, this advantage is more obvious.

These capacitance characteristics have direct impacts on the switching performance of power semiconductor devices: the stronger capacitance nonlinearity of MOSFETs gives them faster switching speeds in the low voltage region, but may also lead to higher voltage spikes; while the more gradual capacitance characteristics of IGBTs help reduce electromagnetic interference during switching processes, but may

lead to higher switching losses.

In summary, the junction capacitance models established in this research successfully capture the key capacitance characteristics of MOSFETs and IGBTs, providing a solid foundation for high-precision dynamic simulation of power electronic systems. In particular, we verified the superiority of the NLM method in power semiconductor device capacitance modeling, which has important value for improving the numerical stability of complex system simulations.

4.3 Double Pulse Test Results

The Nonlinear Mapping (NLM) and Simple Derivative Implementation (SDI) capacitance modeling methods show significant differences in IGBT turn-off characteristic simulation. The double pulse test waveforms in Figure 4.6(b) show that under the NLM model, the current falling edge exhibits longer time characteristics with smooth transitions; while in Figure 4.6(d), the current under the SDI model falls more steeply and rapidly. This time difference directly originates from the essential difference in how the two methods handle capacitance nonlinear characteristics. From Figure 4.6(a), it can be seen that the NLM method processes the capacitance-voltage relationship through mapping functions, making the gate-collector capacitance (C_{gc}) change smoothly with voltage, with good charge transfer continuity and mild Miller effect; while Figure 4.6(c) shows that the SDI method exhibits obvious segmentation characteristics in key transition regions, with enhanced feedback coupling in specific voltage intervals.

From a carrier dynamics perspective, these two modeling methods reflect different physical process emphases. The NLM method has a stable carrier clearance process, continuous charge storage region simulation, exhibiting smoother tail current decay, suitable for steady-state working condition simulation; the SDI method more accurately captures the rapid extraction process of carriers and the dynamics of space charge region expansion, more directly reflecting transient characteristics in real physical processes. This difference is particularly evident in the voltage-current interaction relationship in double pulse test waveforms: under the SDI model, the coupling between gate voltage and current changes is tighter, with current decrease showing stronger correlation with gate voltage changes.

From an application perspective, these two capacitance implementation methods have distinctly different impacts on switching loss calculation, electromagnetic interference prediction, and thermal performance evaluation. The NLM method, with its smooth curves, has good stability in integral calculations, suitable for system-level long-time simulation and thermal cycling simulation; but may underestimate cross-conduction risks under certain extreme conditions. The SDI method can more accurately capture transient peak losses and critical state characteristics, providing more realistic loss predictions under edge working conditions, suitable for in-depth research on device physical characteristics. From the double pulse test results, the SDI model predicts faster turn-off speeds, which may lead to higher dv/dt stress but at the same time bring lower turn-off loss estimates.

Choosing the appropriate capacitance implementation method should balance computational efficiency and physical accuracy, while considering specific application needs. For optimizing drive circuits and gate protection designs, the SDI model may provide more accurate transient characteristic predictions; while for system-level EMI evaluation and long-term stability analysis, the NLM model may be more suitable. The time difference in current falling edges exhibited by these two models in double pulse testing

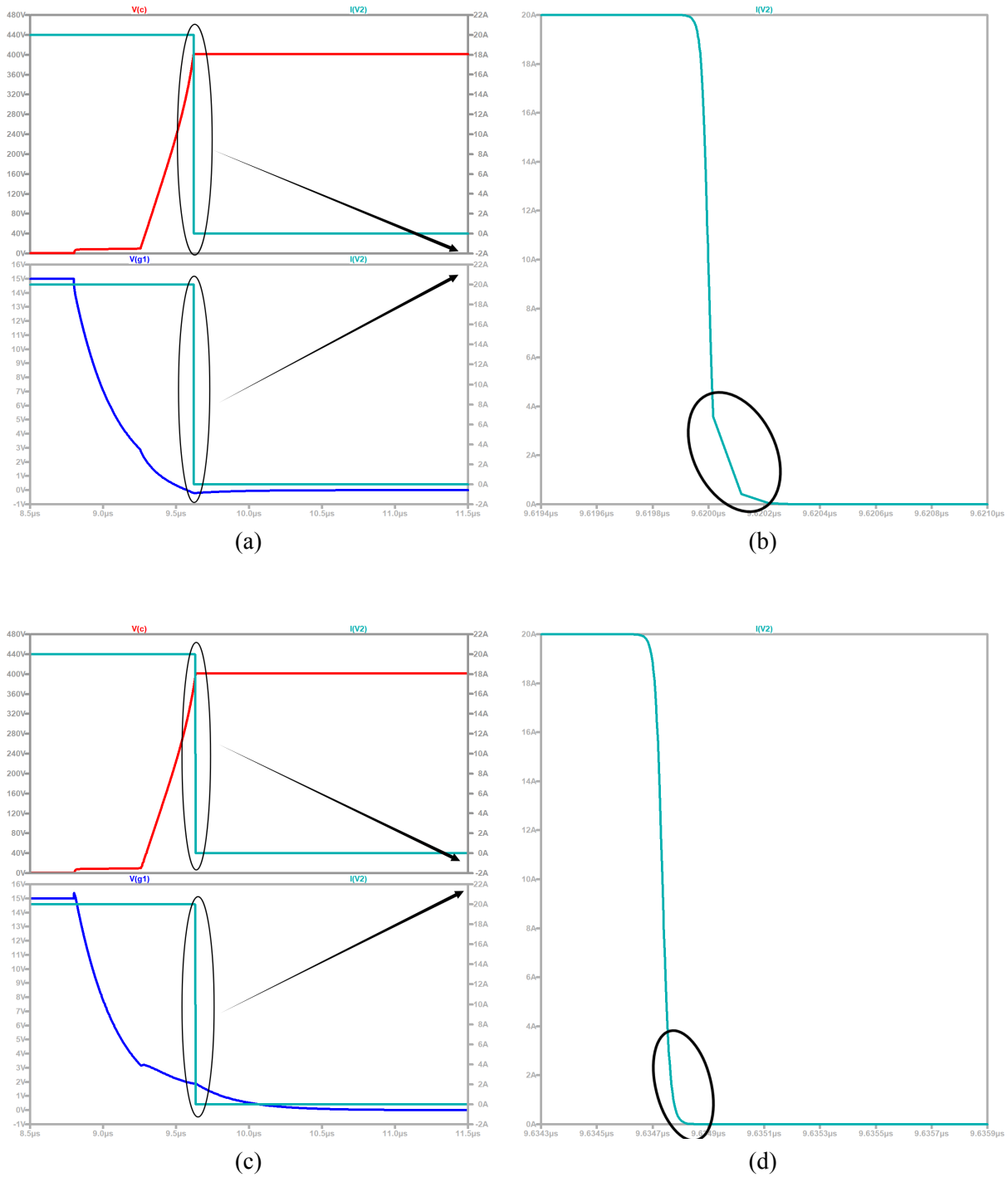


Figure 4.6: Double pulse test results comparing NLM and SDI capacitance modeling methods: (a) switching waveform with NLM method during first turn-off, (b) NLM current falling edge detail showing smooth transitions, (c) switching waveform with SDI method during first turn-off, and (d) SDI current falling edge detail exhibiting steeper characteristics.

is an important reference basis for evaluating the dynamic performance of power conversion systems.

5 Conclusion and Recommendations

This research set out to develop improved modeling methods for power semiconductor devices, with a particular focus on enhancing the accuracy of IGBT models in the low-voltage region. This final chapter summarizes the key findings, discusses their implications, acknowledges limitations, and proposes directions for future research.

5.1 Research Purpose and Key Findings

The primary aim of this research was to create accurate and portable wide-bandgap semiconductor SPICE behavioral models that overcome the limitations of existing approaches. The study focused on developing a correction method based on transfer characteristics to improve the fitting accuracy of IGBT static models in the low-voltage region while maintaining mathematical simplicity and physical reasonableness.

The key findings of this research include:

1. **Effectiveness of the Transfer Characteristic Correction Method**: The proposed method achieved significant improvements in IGBT model accuracy, particularly in the low-voltage region. The average fitting accuracy improved by 12.6% in the MATLAB environment and 21.7% in the circuit simulator. Most notably, under specific gate voltage conditions ($V_{ge} = 4.5V$), improvements of up to 77.9% were observed, demonstrating a qualitative leap in the model's ability to describe IGBT behavior near threshold voltage.
2. **Device-Specific Response to Correction Methods**: A striking difference was observed in how MOSFETs and IGBTs respond to the same correction method. While IGBTs showed dramatic improvements in fitting accuracy in the low-voltage region, MOSFETs exhibited only marginal improvements (1.83%). This finding confirms our theoretical analysis regarding the fundamental structural differences between these devices.
3. **Physical Mechanisms Explaining Different Responses**: The research identified that the composite structure of IGBTs (MOSFET+BJT) and their minority carrier injection mechanism make them significantly more sensitive to transfer characteristic parameter corrections. The dual conduction of electrons and holes in IGBTs creates complex carrier loops and an "electron-hole plasma" region that strongly influences their behavior in the low-voltage region.
4. **Comparative Analysis of Capacitance Modeling Methods**: The study demonstrated that while both NLM and SDI methods can effectively model junction capacitance characteristics, the NLM method exhibits better numerical stability, especially in low voltage regions and fast-changing signal environments. This advantage is particularly evident for composite structure devices like IGBTs.
5. **Double Pulse Test Validation**: Dynamic testing revealed that different capacitance implementation methods have distinct impacts on switching loss calculation, electromagnetic interference prediction, and thermal performance evaluation. The NLM method, with its smooth curves, showed good stability in integral calculations suitable for system-level long-time simulation, while the SDI method more accurately captured transient peak losses and critical state characteristics.

These findings collectively validate the effectiveness of our proposed correction method and provide a deeper understanding of the physical mechanisms that underlie the different behaviors of MOSFETs and IGBTs, particularly in transition regions.

5.2 Theoretical and Practical Implications

The results of this research have several important implications for both theoretical understanding and practical applications in power electronics:

5.2.1 Theoretical Implications

1. **Enhanced Understanding of Device Physics**: This research advances our understanding of how the underlying physical structures of power semiconductor devices influence their electrical behavior. The identification of the specific mechanisms responsible for different responses to modeling corrections enriches the theoretical foundation of semiconductor device physics.
2. **Bridge Between Modeling Approaches**: The study successfully bridges the gap between physics-oriented and mathematics-oriented modeling approaches, demonstrating that targeted mathematical corrections informed by physical insights can significantly improve model accuracy while maintaining computational efficiency.
3. **Nonlinear Behavior in Transition Regions**: The research provides new insights into the nonlinear behavior of power devices in transition regions, particularly the complex interaction between gate control and minority carrier dynamics in IGBTs. This contributes to the theoretical understanding of semiconductor device operation in these critical regions.

5.2.2 Practical Implications

1. **Improved Simulation Accuracy**: The enhanced models developed in this research enable more accurate simulation of power electronic systems, particularly in soft switching and partial conduction application scenarios. This can lead to more efficient design processes and reduced development costs.
2. **Optimized Device Selection**: Better understanding of device-specific behaviors allows engineers to make more informed decisions when selecting power semiconductor devices for specific applications, considering the trade-offs between switching speed, conduction losses, and other parameters.
3. **Enhanced Power Converter Design**: More accurate models, especially in the low-voltage region, enable better prediction of device behavior in critical operating conditions, leading to improved power converter designs with enhanced efficiency, reliability, and electromagnetic compatibility.
4. **Capacitance Implementation Strategy Selection**: The comparative analysis of NLM and SDI methods provides practical guidance for engineers to select the most appropriate capacitance implementation strategy based on their specific requirements for computational efficiency, numerical stability, and physical accuracy.

These implications highlight the significant contribution of this research to both the theoretical understanding and practical application of power semiconductor device modeling.

5.3 Limitations of the Study

While this research has made significant contributions to the field of power semiconductor device modeling, several limitations should be acknowledged:

1. **Device Range Limitations**: The research focused primarily on one specific MOSFET (WOLFSPEED C2M0080120D) and IGBT models based on TCAD simulation data. While this approach provided a controlled environment for comparison, it limits the generalizability of the findings to other device types, voltage classes, or manufacturers.
2. **Temperature Dependency**: Although the study addressed temperature effects in the static part test circuit setup, comprehensive investigation of temperature dependency across the full operating range was beyond the scope of this research. Power semiconductor devices exhibit significant temperature-dependent behavior, particularly IGBTs with their minority carrier dynamics.
3. **Parasitic Effects**: The research primarily focused on intrinsic device characteristics and simplified some parasitic effects that occur in real-world applications. Packaging-related parasitic inductances and resistances, which can significantly impact dynamic behavior, were not fully incorporated into the models.
4. **Validation Method Limitations**: While double pulse testing is a standard method for characterizing switching performance, it represents an idealized switching condition that may not fully capture device behavior in complex converter topologies with multiple switching events and resonant circuits.
5. **Computational Efficiency Analysis**: Although the research compared different implementation methods, a comprehensive quantitative analysis of computational efficiency across different simulation platforms and circuit complexities was not conducted.
6. **New Device Technologies**: The research focused on silicon carbide MOSFETs and traditional IGBTs. Emerging wide bandgap technologies such as gallium nitride (GaN) devices, which may exhibit different physical behaviors and modeling requirements, were not addressed.

These limitations represent opportunities for future research to extend and refine the modeling approaches developed in this study.

5.4 Recommendations for Future Research

Based on the findings and limitations of this study, several promising directions for future research are identified:

1. **Extension to Wider Device Range**: Future research should extend the application of the transfer characteristic correction method to a broader range of power semiconductor devices, including different voltage and current ratings, manufacturing technologies, and device families. This would help establish the generalizability of the approach and potentially reveal additional device-specific optimization opportunities.
2. **Enhanced Temperature-Dependent Modeling**: Developing more comprehensive temperature-dependent models that incorporate the effects of temperature on both static and dynamic character-

istics would be valuable. This could include detailed modeling of minority carrier lifetime variation with temperature in IGBTs and its impact on tail current characteristics.

3. **Integration with Parasitic Extraction Tools**: Combining the improved device models with advanced parasitic extraction tools would create more realistic system-level simulations. This integration could address the complex interactions between device behavior and circuit parasitics, particularly in high-frequency applications.
4. **Advanced Validation Techniques**: Developing more sophisticated validation techniques that can isolate and quantify individual aspects of device behavior would enhance model verification. This might include specialized test circuits for specific physical phenomena or novel measurement techniques for hard-to-observe internal device dynamics.
5. **Machine Learning Enhancement**: Exploring the application of machine learning algorithms to further refine parameter extraction and model optimization could improve both accuracy and computational efficiency. Hybrid approaches combining physics-based models with data-driven methods may offer the best of both worlds.
6. **Application to Emerging Technologies**: Extending the modeling approach to emerging technologies such as GaN devices, silicon-carbide super-junction MOSFETs, and new IGBT structures would ensure the relevance of the research to future power electronic systems.
7. **Multi-Physics Integration**: Developing more integrated multi-physics models that simultaneously address electrical, thermal, and reliability aspects would provide a more holistic approach to power device modeling. This could include aging effects and reliability predictions based on operating conditions.
8. **Standardization Efforts**: Contributing to standardization efforts for power semiconductor device modeling would help ensure wider adoption of improved modeling approaches across the industry. This could include developing standard parameter extraction procedures and model validation benchmarks.
9. **Real-Time Simulation Optimization**: Optimizing the models for real-time simulation applications, such as hardware-in-the-loop testing of power electronic controllers, would enhance their practical utility in advanced development workflows.

These recommendations address both the specific limitations identified in this study and broader opportunities to advance the field of power semiconductor device modeling.

5.5 Summary

This research has made significant contributions to the field of power semiconductor device modeling by developing and validating an improved approach for modeling MOSFETs and IGBTs, with particular emphasis on enhancing accuracy in the critical low-voltage transition region. The study was motivated by the recognition that existing models, while effective in many respects, face challenges in accurately representing the nonlinear characteristics of power devices, especially IGBTs, in this operationally important region.

The core innovation of this research lies in the development of a correction method based on transfer characteristics, which significantly improved the fitting accuracy of IGBT models in the low-voltage region while maintaining mathematical simplicity and physical reasonableness. Through comprehensive theoretical analysis and experimental verification, the research revealed that IGBTs, due to their composite structure and minority carrier injection mechanisms, are significantly more sensitive to transfer characteristic corrections than MOSFETs. This finding not only validates the effectiveness of the proposed method but also deepens our understanding of the fundamental physical differences between these device types.

The research also conducted a detailed comparative analysis of two major capacitance modeling methods—Nonlinear Mapping (NLM) and Simple Derivative Implementation (SDI)—revealing their respective advantages in different application scenarios. This comparison provides valuable guidance for engineers in selecting appropriate modeling strategies based on their specific requirements for numerical stability, computational efficiency, and physical accuracy.

The effectiveness of the proposed models was validated through comprehensive simulation and testing, including static characteristic fitting analysis and dynamic double pulse testing. The results demonstrated that the enhanced models can significantly improve the accuracy of power electronic system simulations, particularly in critical operating conditions such as soft switching and partial conduction scenarios.

Beyond its methodological contributions, this research has advanced our theoretical understanding of power semiconductor device physics, particularly the complex interactions between gate control and minority carrier dynamics in IGBTs. It has also provided practical insights that can inform device selection, circuit design, and system optimization in a wide range of power electronic applications.

While acknowledging certain limitations related to the scope of devices tested, temperature dependencies, and parasitic effects, this research has laid a solid foundation for future studies. Promising directions for extending this work include broadening the device range, enhancing temperature-dependent modeling, integrating parasitic effects, exploring machine learning enhancements, and applying the approach to emerging wide bandgap technologies.

In conclusion, this research represents a significant step forward in bridging the gap between physics-oriented and mathematics-oriented approaches to semiconductor device modeling. By improving the accuracy of power device models, particularly in transition regions, this work contributes to the advancement of power electronics technology across diverse applications, from renewable energy systems to electric vehicles and industrial automation.

BIBLIOGRAPHY

[1] B. W. Nelson, A. N. Lemmon, S. J. Jimenez, H. A. Mantooth, B. T. DeBoi, C. D. New, and M. M. Hossain, "Computational efficiency analysis of SiC MOSFET models in SPICE: Dynamic behavior," *IEEE Open Journal of Power Electronics*, vol. 2, pp. 106–123, 2021.

[2] H. Miyake *et al.*, "Comprehensive parameter extraction procedure for advanced IGBT model with electro-thermal features," in *IEEE International Reliability Physics Symposium*, 2013, pp. 5D.1.1–5D.1.6.

[3] S. Koziel, L. Leifsson, and X. S. Yang, "Surrogate-based modeling and optimization: Application in engineering." Springer Science & Business Media, 2015.

[4] M. A. Islam, K. Rahman, and N. Rahim, "Predicting lifetime of semiconductor power devices under power cycling stress using artificial neural network," *IEEE Transactions on Power Electronics*, vol. 37, no. 6, pp. 7124–7135, 2022. [Online]. Available: https://doi.org/10.1109/JESTPE.2022.3194189

[5] L. W. Nagel and D. Pederson, "Spice (simulation program with integrated circuit emphasis)," University of California, Berkeley, Tech. Rep. UCB/ERL M382, April 1973.

[6] Y. Tsividis, *Operation and Modeling of the MOS Transistor*, 2nd ed. New York, NY: Oxford University Press, 1999.

[7] W. Liu, X. Jin, X. Xi, J. Chen, M.-C. Jeng, Z. Liu, Y. Cheng, K. Chen, M. Chan, K. Hui, J. Huang, R. Tu, P. K. Ko, and C. Hu, *BSIM3v3 Manual (Version 3.3)*, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA, 1996, technical documentation.

[8] C. C. Enz and E. A. Vittoz, *Charge-Based MOS Transistor Modeling: The EKV Model for Low-Power and RF IC Design*. Chichester, UK: John Wiley & Sons, Ltd, 2006, print ISBN: 9780470855416, Online ISBN: 9780470855461.

[9] A. Hefner and D. Blackburn, "Thermal component models for electro-thermal network simulations," in *[1993 Proceedings] Ninth Annual IEEE Semiconductor Thermal Measurement and Management Symposium*, 1993, pp. 88–98.

[10] R. Kraus and A. Mattausch, "Status and trends of power semiconductor device models for circuit simulation," *IEEE Transactions on Power Electronics*, vol. 13, no. 3, pp. 452–465, 1998.

[11] T. R. McNutt and A. R. Hefner, "A unified SiC power MOSFET model for circuit simulation," in *Proceedings of the 36th Power Electronics Specialists Conference*, 2005, pp. 331–337.

[12] Z. Chen, "Characterization and modeling of high-switching-speed behavior of SiC active devices," Master's thesis, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, 2009. [Online]. Available: https://vtechworks.lib.vt.edu/items/1c365e85-f7dc-4d2a-a201-75380e50e98e

[13] K. Chen, Z. Zhao, L. Yuan, T. Lu, and F. He, "The impact of nonlinear junction capacitance on switching transient and its modeling for sic mosfet," *IEEE Transactions on Electron Devices*, vol. 62, no. 2, pp. 333–338, 2015.

[14] I. Almpanis, P. Evans, K. Li, and N. Lophitis, “Igbt model for circuit simulations: Implementation of the nonlinear voltage-and current-dependent capacitance method to silicon igbts,” in *2024 IEEE Design Methodologies Conference (DMC)*, 2024, pp. 1–3.

[15] G. Wiedemann, T. Lamm, and R. Schacht, “Transient electro-thermal characterisation at systemlevel for an easypack-igbt-module – reduced order modelling (rom) and junction temperature evaluation based on the onstate resistance,” in *2024 30th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2024, pp. 1–8.

[16] S. Perez, R. M. Kotecha, A. U. Rashid, M. M. Hossain, T. Vrotsos, A. M. Francis, H. A. Mantooth, E. Santi, and J. L. Hudgins, “A datasheet driven unified si/sic compact igbt model for n-channel and p-channel devices,” *IEEE Transactions on Power Electronics*, vol. 34, no. 9, pp. 8329–8341, 2019.

[17] F. Mihalic, K. Jezernik, K. Krischan, and M. Rentmeister, “Igbt spice model,” *IEEE Transactions on Industrial Electronics*, vol. 42, no. 1, pp. 98–105, 1995.

[18] X. Huang, Q. Li, Z. Liu, and F. C. Lee, “Analytical loss model of high voltage gan hemt in cascode configuration,” in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 3587–3594.

[19] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. New York, NY: Springer, 2008.

[20] M. Liang, T. Zheng, and Y. Li, “An improved analytical model for predicting the switching performance of SiC MOSFETs,” *Journal of Power Electronics*, vol. 16, no. 1, pp. 374–387, 2016.

[21] G. Verneau, L. Aubard, J.-C. Crébier, C. Schaeffer, and J.-L. Schanen, “Empirical power MOSFET modeling: Practical characterization and simulation implantation,” in *37th IAS Annual Meeting. Conference Record of the Industry Applications Conference*, vol. 4, 02 2002, pp. 2425–2432.

[22] B. J. Baliga, *The IGBT Device: Physics, Design and Applications of the Insulated Gate Bipolar Transistor*. William Andrew Publishing/Elsevier, 2015.

[23] M. Trivedi and K. Shenai, “Comparison of RF performance of vertical and lateral DMOSFET,” in *11th International Symposium on Power Semiconductor Devices and ICs. ISPSD’99 Proceedings (Cat. No.99CH36312)*, 1999, pp. 245–248.

[24] Y. Yang, Z. Zhao, C. Peng, X. Li, Z. Sun, and X. Cui, “An improved behavioral model for high-voltage and high-power igbt chips,” *CSEE Journal of Power and Energy Systems*, vol. 9, no. 1, pp. 284–292, 2023.

[25] H. Jeong, S. Woo, J. Choi, H. Cho, Y. Kim, and J. Kong, “Fast and expandable ann-based compact model and parameter extraction for emerging transistors,” *IEEE Journal of the Electron Devices Society*, vol. 11, pp. 153–160, 2023. [Online]. Available: https://doi.org/10.1109/JEDS.2023.3246477

[26] D. Navarro, M. Miyake, and T. Matsumoto, “A sequential model parameter extraction technique for physics-based igbt compact models,” *IEEE Transactions on Electron Devices*, vol. 60, no. 2, pp. 580–586, 2013. [Online]. Available: https://doi.org/10.1109/TED.2012.2226724

[27] Y. Mukunoki, K. Konno, T. Matsuo, T. Horiguchi, A. Nishizawa, M. Kuzumoto, M. Hagiwara, and H. Akagi, “An improved compact model for a Silicon-Carbide MOSFET and its application to accurate circuit simulation,” *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9834–9842, 2018.

[28] M. Riccio, V. d'Alessandro, G. Romano, L. Maresca, G. Breglio, and A. Irace, "A temperature-dependent SPICE model of SiC power MOSFETs for within and out-of-SOA simulations," *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 8020–8029, 2018.

[29] Y. Mukunoki, T. Horiguchi, Y. Nakayama, A. Nishizawa, Y. Nakamura, K. Konno, M. Kuzumoto, and H. Akagi, "Modeling of a silicon-carbide mosfet with focus on internal stray capacitances and inductances, and its verification," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 2671–2677.

[30] I. Zeltser and S. Ben-Yaakov, "On SPICE simulation of voltage-dependent capacitors," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 3703–3710, 2018.

[31] Z. Duan, T. Fan, X. Wen, and D. Zhang, "Improved SiC power MOSFET model considering nonlinear junction capacitances," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2509–2517, 2018.

[32] M. Meisser, T. Blank, K. Bendel, R. Reuter, and K. Schubert, "Design and implementation of a low inductive sic-module and test-bench for characterization of next generation power semiconductors," in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, pp. 4325–4330.

[33] E. Hoene, A. Ostmann, B. Lai, C. Marczok, and A. Müsing, "Ultra-low-inductance power module for fast switching semiconductors," *CIPS 2013 - 8th International Conference on Integrated Power Electronics Systems*, pp. 198–205, 01 2013, proceedings of CIPS 2013.

[34] D. Nayak, Y. Ravi Kumar, and S. Pramanick, "A comparative study of loss measurement techniques for sic mosfet based pe converters," in *IECON 2022 – 48th Annual Conference of the IEEE Industrial Electronics Society*, 2022, pp. 1–6.

[35] J. Wang, H. S.-h. Chung, and R. T.-h. Li, "Characterization and experimental assessment of the effects of parasitic elements on the mosfet switching performance," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 573–590, 2013.

[36] N. Haleem, A. Rajapakse, and A. Gole, "Improved circuit model for simulating igbt switching transients in vscs," *Journal of Power Electronics*, vol. 18, no. 6, pp. 1901–1911, 11 2018.

[37] B. Dwiza and K. Jayaraman, "Analytical approach for common mode emi noise analysis in dual active bridge converter," in *2020 IEEE 46th Annual Industrial Electronics Society Conference (IECON)*, 10 2020, pp. 1279–1284.

[38] Y. Guo, H. Wang, and B. Xie, "An end-to-end ai-based automated process for semiconductor device parameter extraction," *IEEE Transactions on Electron Devices*, vol. 69, no. 6, pp. 3217–3224, 2022. [Online]. Available: https://doi.org/10.1109/TED.2022.3165567

[39] T. H. Duong, R. Rivera, and A. Hefner, "Parameter extraction and optimization for gan hemts using a physics-based compact model," in *2014 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2014, pp. 1–4. [Online]. Available: https://doi.org/10.1109/CSICS.2014.6978561

[40] J. Zhang, W. Liu, and M. Chen, "Remaining useful life prediction of power mosfets using model-based and data-driven methods," *IEEE Transactions on Device and Materials Reliability*, vol. 23, no. 2, pp. 278–288, 2023. [Online]. Available: https://doi.org/10.1109/TDMR.2023.3257894

[41] T. Heckel and L. Frey, “A novel charge based spice model for nonlinear device capacitances,” in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2015, pp. 141–146.

[42] A. Endruschat, T. Heckel, D. Platz, and C. Unger, “Modeling power MOSFETs with a modified capacitance model in SPICE,” in *2009 13th European Conference on Power Electronics and Applications*, 2009, pp. 1–10.

APPENDICES

APPENDIX I

Circuit Netlists

I.1 Static Model Test Circuits

I.1.1 MOSFET Static Model Test Circuits

I.1.1.1 C2M0080120D Static Model Test Circuit

Listing I.1: C2M0080120D Static Model Test Circuit

```
* SiC MOSFET DC Analysis
* Using C2M0080120D model
* Device definition
XU1 d g 0 N001 N001 C2M0080120D
* Sources
vds d 0 10   ; Drain-Source voltage
Vgs g 0 20   ; Gate-Source voltage
VT N001 0 25 ; Temperature control voltage
* Analysis commands
.dc VDS 0 12.5v 5mv
+VGS list 20v 18v 16v 14v 12v 10v 8v 6v 4v 2v 0v
.temp 25
* Include model library
.include C2M0080120D.lib
.backanno
.end
```

I.1.1.2 SiC MOSFET Static Model Test Circuit

Listing I.2: SiC MOSFET Static Model Test Circuit

```
* Using CD4001B/CD4011 model
* Device: SiC MOSFET
* NXP g & h (NM) 3301 CD4001B/CD11
* Rev 0.75
* Vgs g 0 20           Gate Source voltage
* Vds d 0 10           Drain Source voltage
* Include model library
* Analysis
Vgs g 0 20
Bosfet_static P001 P002
i={a(v(g,0))-a(v(g,0))/(1+(v(d,0)/b(v(g,0)))**c(v(g,0)))}
vds d 0 10
R1 P001 0 1
R2 out P002 1k
.dc VDS 0 1000v 5mv VGS list 0v 2v 4v 6v 8v 10v 12v 14v 16v 18v 20v
```

```
.func a(vgs)=sa1/(1+((vgs-5)/sa2)**sa3)+sa4
.param sa1=7100 sa2=67877 sa3=2186 sa4=1.06
.temp 25
.func b(vgs)=sb1/(1+((vgs-5)/sb2)**sb3)+sb4
.param sb1=17349 sb2=50861 sb3=0.25 sb4=55305
.func c(vgs)=sc1/(1 + ((vgs-5)/sc2)**sc3)+sc4
.param sc1=1.187 sc2=4.25 sc3=2.4375 sc4=0.4666
.backanno
.end
```

I.1.2 IGBT Static Model Test Circuits

I.1.2.1 Original IGBT Model Circuit

Listing I.3: Original IGBT Model Circuit

```
* Using IGBT model
* Device: Power IGBT
* Forward characteristics simulation model
* Rev 1.0
* Vge g 0 20           Gate Emitter voltage
* Vce c 0 10           Collector Emitter voltage
* Include model library
* Analysis
Vge g 0 20
Bgbt_static P001 P002
i={a(v(g,0))-a(v(g,0))/(1+(v(c,0)/b(v(g,0)))**c(v(g,0)))}
vce c 0 10
R1 P001 0 1
R2 out P002 1k
.dc VCE 0 20v 5mv VGE list 0v 4.5v 6.5v 9.5v 11.5v 13.5v 15.5v
.func a(vge)=sa1/(1+((vge-3)/sa2)**sa3)+sa4
.param sa1=-170637.513467 sa2=35.507056 sa3=1.639279 sa4=170621.727206
.temp 25
.func b(vge)=sb1/(1+((vge-3)/sb2)**sb3)+sb4
.param sb1=-5.608560 sb2=9.947009 sb3=1.161004 sb4=6.687413
.func c(vge)=sc1/(1 + ((vge-3)/sc2)**sc3)+sc4
.param sc1=2.463954 sc2=3.056347 sc3=2.092181 sc4=3.094157
.backanno
.end
```

I.1.2.2 Enhanced IGBT Model with Transfer Characteristic Correction

Listing I.4: Enhanced IGBT Model with Transfer Characteristic Correction

```
* Using enhanced IGBT model with nonlinear correction
* Device: Power IGBT with improved transition region modeling
* Forward characteristics with Vce-dependent parameter correction
* Rev 1.0
* Vge g 0 20           Gate Emitter voltage
```

```
* Vce c 0 10           Collector Emitter voltage
* Include model library
* Analysis
Bgbt_static_fix P001 P002 I=original_model(v(p5),v(p6))
R1 out P002 1k
R2 P001 0 1
vce c 0 10
vge g 0 20
.func a(vge)=sa1/(1+((vge-vth)/sa2)**sa3)+sa4
.param sa1=-178387 sa2=40 sa3=1.39 sa4=179359
.func b(vge,vce)=(sb1/(1+((vge-vth)/sb2)**sb3)+sb4)*(1+kb*exp(-alpha_b*vce))
.param sb1=-3.83 sb2=6.399 sb3=1.34 sb4=5.486
.param kb=1.9989 alpha_b=5.467
.func c(vge,vce)=(sc1/(1 + ((vge-vth)/sc2)**sc3)+sc4)+kc*(1-1/(1+exp(-alpha_c*(vce-beta_c)
)))
.param sc1=1.1 sc2=4.06 sc3=9.98 sc4=3.18
.param kc=1.05 alpha_c=5.001 beta_c=1.2
.param Vth=4.5
.func original_model(vge,vce) {(a(vge)-a(vge)/(1+(vce/b(vge,vce))**c(vge,vce)))}
.dc VCE 0 8v 5mv VGE list 0v 4.5v 6.5v 9.5v 11.5v 13.5v 15.5v
.temp 25
.backanno
.end
```

I.2 Capacitance Test Circuits

I.2.1 NLM Implementation Circuits

I.2.1.1 IGBT NLM Capacitance Test Circuit

Listing I.5: IGBT NLM Capacitance Test Circuit

```
Bce1 c 0 I=(Cce_func(V(c,0))/1p-1)*i(VS32)
V1 c 0 SINE({Vce+1} {Vce} 2k 0 0 -90)
C1 g 0 57n
Bce2 Cce_meas 0 V=I(Cce1)/ddt(V(c,0))
Bgc2 Cgc_meas 0 V=I(Cgc1)/ddt(V(g,c))
B1 N001 0 V=v(g,c)
C2 33 N001 1p
VS33 33 0 0
Bgc1 c g I=(Cgc_func(V(c,0))/1p-1)*i(VS33)
B2 N002 0 V=V(c,0)
C3 32 N002 1p
VS32 32 0 0
V2 g 0 0
.tran 0 200u 0 1n
.meas TRAN Cce FIND V(Cce_meas) AT 100u
.meas TRAN Cgc FIND V(Cgc_meas) AT 100u
.inc "C:\Users\ADMIN\Documents\LTspice\Cce_fixvce_20.txt"
.inc "C:\Users\ADMIN\Documents\LTspice\Cgc_fixvce_20.txt"
```

```
.step param Vce 0 400 2
.backanno
.end
```

I.2.1.2 MOSFET NLM Capacitance Test Circuit

Listing I.6: MOSFET NLM Capacitance Test Circuit

```
Bds1 d 0
I=((451.2059/(1+(V(d,0)/27.3671)**(0.9577))+452.4872*exp(-0.1747*V(d,0))+2127.8355/(V(d,0)
**0.0467+31.5390))-1)*i(VS32)
V1 d 0 SINE({Vds+1} {Vds} 2k 0 0 0)
C1 g 0 1130p
Bds2 Cds_meas 0 V=I(Cds1)/ddt(V(d,0))
Bgd2 Cgd_meas 0 V=I(Cgd1)/ddt(V(g,d))
V2 g 0 0
Bgd1 d g
I=((701.7634/(1+(V(d,0)/2.6567)**(2.4523))+7.5024+384.0937/(V(d,0)**1.0520+24.5681))-1)*i(
VS33)
VS33 33 0 0
B1 N001 0 V=v(g,d)
C2 33 N001 1p
VS32 32 0 0
B2 N002 0 V=V(d,0)
C3 32 N002 1p
.tran 0 200u 0 1n uic
.meas TRAN Cds MAX V(Cds_meas) FROM 0 TO 23.2u
.meas TRAN Cgd MAX V(Cgd_meas) FROM 0 TO 23.2u
.step param Vds 0 200 2
.backanno
.end
```

I.2.2 SDI Implementation Circuits

I.2.2.1 IGBT SDI Capacitance Test Circuit

Listing I.7: IGBT SDI Capacitance Test Circuit

```
Bgc1 g c I=Cgc_func(V(c,0))*ddt(V(g,c))
Bce1 c 0 I=Cce_func(V(c,0))*ddt(V(c,0))
V1 c 0 SINE({Vce+1} {Vce} 2k 0 0 -90)
C1 g 0 57n
Bce2 Cce_meas 0 V=I(Cce1)/ddt(V(c,0))
Bgc2 Cgc_meas 0 V=I(Cgc1)/ddt(V(g,c))
V2 g 0 0
.tran 0 200u 0 1n
.meas TRAN Cce FIND V(Cce_meas) AT 100u
.meas TRAN Cgc FIND V(Cgc_meas) AT 100u
.inc "C:\Users\ADMIN\Documents\LTspice\Cce_fixvce_20.txt"
.inc "C:\Users\ADMIN\Documents\LTspice\Cgc_fixvce_20.txt"
```

```
.step param Vce 0 400 2
.backanno
.end
```

I.2.2.2 MOSFET SDI Capacitance Test Circuit

Listing I.8: MOSFET SDI Capacitance Test Circuit

```
Bds1 d 0
I=(451.2059/(1+(V(d,0)/27.3671)**(0.9577))+452.4872*exp(-0.1747*V(d,0))+2127.8355/(V(d,0)
**0.0467+31.5390))*1p*ddt(V(d,0))
V1 d 0 SINE({Vds+1} {Vds} 2k 0 0 0)
C1 g 0 1130p
Bds Cds_meas 0 V=I(Cds1)/ddt(V(d,0))
Bgd Cgd_meas 0 V=I(Cgd1)/ddt(V(d,g))
V2 g 0 0
Bgd1 d g
I=(701.7634/(1+(V(d,0)/2.6567)**(2.4523))+7.5024+384.0937/(V(d,0)**1.0520+24.5681))*1p*ddt
(V(d,g))
.tran 0 200u 0 1n uic
.meas TRAN Cds MAX V(Cds_meas) FROM 0 TO 23.2u
.meas TRAN Cgd MAX V(Cgd_meas) FROM 0 TO 23.2u
.step param Vds 0 200 2
.backanno
.end
```

I.3 Double Pulse Test Circuits

I.3.1 IGBT NLM Double Pulse Test Circuit

Listing I.9: IGBT NLM Double Pulse Test Circuit

```
* C:\Users\ADMIN\Desktop\cap_ltspice\I=20_change_capacitance.asc
B1 c 0
I=pure_subth(V(g,0),V(c,0))*hard_switch(V(g,0))+original_model(V(g,0),V(c,0))*(1-
hard_switch(V(g,0)))
B2 c g1 I=(Cgc_func(V(c,0))/10p-1)*i(VS33)
V1 g 0 PWL(0 0 +1u 0 +1n 15 +7.8u 15 +1n 0 +5u 0 +1n 15 +1u 15)
Cbus1 N001 0 42.3?VDC1 N001 0 400v
C1 g1 0 57n
V2 N006 c 0
B3 c 0 I=(Cce_func(V(c,0))/10p-1)*i(VS32)
I1 N001 N006 20
D1 N006 N001 DNAME
B4 N004 0 V=V(c,0)
C2 N005 N004 10p
VS1 N005 0 0
B5 N002 0 V=v(g,c)
C3 N003 N002 10p
```

```
VS2 N003 0 0
R1 g1 g 5
.model D D
.lib C:\Users\ADMIN\AppData\Local\LTspice\lib\cmp\standard.dio
.func a(vge)=sa1/(1+((vge-3)/sa2)**sa3)+sa4
.param sa1=-141222 sa2=29.79
.func b(vge,vce)=(sb1/(1+((vge-3)/sb2)**sb3)+sb4)*(1+1.047*exp(-7.787*vce))
.param sb1=-5.6 sb2=9.5524
.func c(vge,vce)=(sc1/(1 + ((vge-3)/sc2)**sc3)+sc4)+1.061*(1-1/(1+exp(-5.07*(vce-1.199))))
.param sc1=2.11 sc2=3.78
.temp 25
.tran 0 18us 1ns 0.0001us uic
.param sa3=1.75 sa4=140946
.param sb3=1.25 sb4=6.55
.param sc3=2.518 sc4=3.049
.inc "C:\Users\ADMIN\Documents\LTspice\Cce_fixvce_20.txt"
.inc "C:\Users\ADMIN\Documents\LTspice\Cgc_fixvce_20.txt"
.model DNAME D(IS=1e-14 RS=0.00001 N=1 TT=0 CJO=0 VJ=1 M=0.5 EG=1.11 XTI=3 KF=0 AF=1 FC
=0.5 BV=800 IBV=1e-12)
.options method=trap trtol=7 reltol=1e-10 abstol=1e-10 vntol=1e-7 maxstep=0.5n cshunt=1e
-15
.option plotwinsize=0
.param Vth=3.0 n_subth=1.5 I0=1e-12 Vt=0.026 trans_width=0.1
.func original_model(vge,vce) {(a(vge)-a(vge)/(1+(vce/b(vge,vce))**c(vge,vce)))*limit((vge
-3)/0.1,0,1)}
.func pure_subth(Vge,Vce) {I0*exp((Vge-Vth)/(n_subth*Vt))*(1-exp(-Vce/Vt))*(1+Vge/10)}
.func hard_switch(Vge) {0.5*(1+tanh((Vth-Vge)/trans_width*4))}
.backanno
.end
```

I.3.2 IGBT SDI Double Pulse Test Circuit

Listing I.10: IGBT SDI Double Pulse Test Circuit

```
* C:\Users\ADMIN\Desktop\cap_ltspice\I=20_filtered_1.asc
B1 c 0
I=pure_subth(V(g,0),V(c,0))*hard_switch(V(g,0))+original_model(V(g,0),V(c,0))*(1-
hard_switch(V(g,0)))
B2 c g1 I=Cgc_func(V(c,0))*ddt(V(c,g))
V1 g 0 PWL(0 0 +1u 0 +1n 15 +7.8u 15 +1n 0 +5u 0 +1n 15 +1u 15)
Cbus1 N001 0 42.3?VDC1 N001 0 400v
C1 g1 0 57n
V2 N002 c 0
B3 c 0 I=Cce_func(V(c,0))*ddt(V(c,0))
I1 N001 N002 20
D1 N002 N001 DNAME
R1 g1 g 5
.model D D
.lib C:\Users\ADMIN\AppData\Local\LTspice\lib\cmp\standard.dio
.func a(vge)=sa1/(1+((vge-3)/sa2)**sa3)+sa4
.param sa1=-141222 sa2=29.79
```

```
.func b(vge,vce)=(sb1/(1+((vge-3)/sb2)**sb3)+sb4)*(1+1.047*exp(-7.787*vce))
.param sb1=-5.6 sb2=9.5524
.func c(vge,vce)=(sc1/(1 + ((vge-3)/sc2)**sc3)+sc4)+1.061*(1-1/(1+exp(-5.07*(vce-1.199))))
.param sc1=2.11 sc2=3.78
.temp 25
.tran 0 18us 1ns 0.0001us uic
.param sa3=1.75 sa4=140946
.param sb3=1.25 sb4=6.55
.param sc3=2.518 sc4=3.049
.inc "C:\Users\ADMIN\Documents\LTspice\Cce_fixvce_20.txt"
.inc "C:\Users\ADMIN\Documents\LTspice\Cgc_fixvce_20.txt"
.model DNAME D(IS=1e-14 RS=0.00001 N=1 TT=0 CJO=0 VJ=1 M=0.5 EG=1.11 XTI=3 KF=0 AF=1 FC
=0.5 BV=800 IBV=1e-12)
.option plotwinsize=0
.param Vth=3.0 n_subth=1.5 I0=1e-12 Vt=0.026 trans_width=0.1
.func original_model(vge,vce) {(a(vge)-a(vge)/(1+(vce/b(vge,vce))**c(vge,vce)))*limit((vge
-3)/0.1,0,1)}
.func pure_subth(Vge,Vce) {I0*exp((Vge-Vth)/(n_subth*Vt))*(1-exp(-Vce/Vt))*(1+Vge/10)}
.func hard_switch(Vge) {0.5*(1+tanh((Vth-Vge)/trans_width*4))}
.backanno
.end
```