Cyprus University of Technology

HANGZHOU DIANZI UNIVERSITY

Master's Thesis

Development of a low-cost Micro-PMU (μPMU)

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Limassol, December,2024

MSc in Electronics Science and Technology

CYPRUS UNIVERSITY OF TECHNOLOGY
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Abstract

The proliferation of smart grid technology necessitates widespread deployment of Phasor Measurement Units (PMUs) for enhanced real-time power system monitoring, yet the high cost of traditional commercial PMUs—typically $5,000—hinders their adoption, especially in distribution networks. This paper introduces a low-cost Micro-PMU (μPMU) prototype, leveraging off-the-shelf components like the STM32F407 microcontroller and AD7606 ADC to achieve a total cost of just $100, representing a 80% reduction compared to μPMUs. The system integrates GPS Pulse Per Second (PPS) synchronization with a local clock for precise time-aligned signal sampling, employs a high-precision ADC for data acquisition, and utilizes an Interpolated Discrete Fourier Transform (IPDFT) algorithm optimized for resource-constrained hardware to accurately estimate voltage magnitude and frequency. Its modular design incorporates Tunneling Magnetoresistance (TMR) sensing for non-invasive current measurement, offering high sensitivity and compactness suitable for distribution grid applications. Voltage steady-state experimental results demonstrate compliance with IEEE C37.118.1 standards, achieving 0.78%TVE. Future work will focus on improving the measurement accuracy of TMR current measurement and completing the phase test of current and validating its performance under dynamic grid conditions through field trials, ensuring comprehensive evaluation of synchro phasor accuracy in real-world scenarios, providing a scalable and cost-effective solution to promote synchronized phasor measurement adoption in smart grid infrastructure.

Keywords: μPMU, low-cost, IPDFT, TMR

1. Introduction

Modern power grids face escalating reliability challenges due to the limitations of traditional Phasor Measurement Units (PMUs). Conventional PMUs, while critical for wide-area monitoring in transmission networks, are prohibitively expensive (typically exceeding $2500 per unit) and sparsely deployed in distribution grids. This cost-density imbalance creates persistent "blind spots" in real-time situational awareness, leaving distribution networks vulnerable to cascading failures. Historical blackouts, such as the 1965 Northeast Blackout in the United States and the 2003 Northeast Blackout affecting the U.S. and Canada[错误!未定义书签。] triggered by undetected local faults, underscore the catastrophic consequences of inadequate monitoring. Despite advancements in grid automation, the lack of cost-effective, high-accuracy measurement tools at the distribution level remains a critical research gap, hindering proactive fault detection and resilience enhancement.

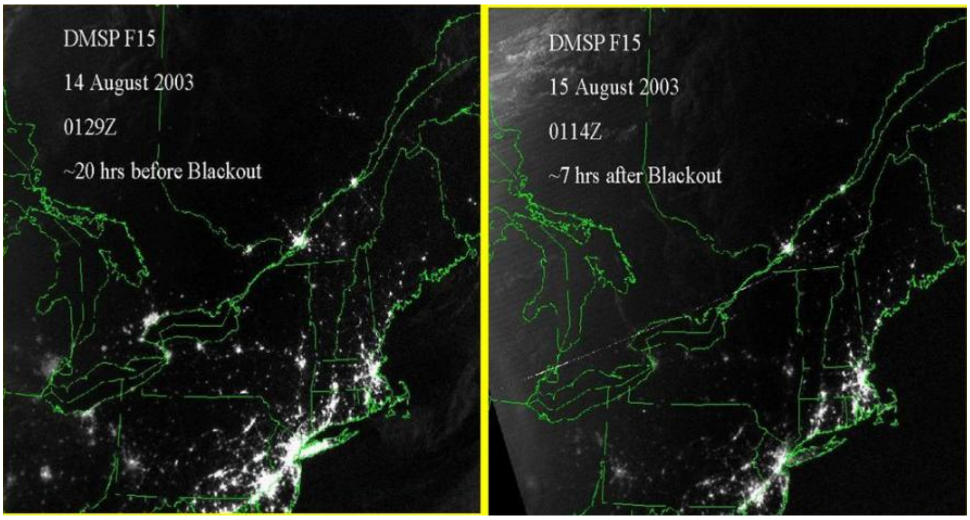

Figure 1.1 2003 North American Blackout

As shown in the Figure1.1, the light spots in the right - hand figure are significantly reduced, with many areas plunging into darkness, indicating that many lights went out after the power outage occurred.

This study posits that PMU architecture integrating commercial off-the-shelf (COTS) components with phasors measurement algorithms can achieve industrial-grade phasor measurement accuracy (Total Vector Error, TVE <1%) at 20% of the cost of traditional PMUs. By resolving the cost-accuracy trade-off, this approach directly addresses the monitoring gaps that contributed to historical grid failures. For instance, the proposed µPMU's low-cost design enables dense deployment at distribution nodes, enhancing fault prediction capabilities and mitigating cascading outage risks.

Traditional PMU
size：30cm×17.7cm×48.3cm
price：5000 $

µPMU
size：12.8cm ×5.5cm×9.5cm
price：500 $

Figure 1.2 Comparison of PMU and μPMU

As shown in the Figure1.2 traditional PMUs provide high-accuracy measurements, their higher costs and larger in size make them impractical for resource-constrained environments. µPMUs, by contrast, reduce hardware complexity and cost, making them easier to deploy across existing grid infrastructure and reducing the risk of power outages.

This research aims to design a µPMU hardware architecture using commercial off --the- shelf (COTS) components, with the goal of reducing the unit cost to $500. The hardware architecture integrates phasor calculation algorithms and intelligent communication functions. This framework ensures achieving a frequency estimation error below 0.005Hz, an amplitude measurement error within 1%, and a phase angle error under 1°. While the current design prioritizes affordability and core functionalities, TVE (Total Vector Error) cannot be measured at the same time due to hardware resource constraints.

The successful deployment of micro-PMUs carries profound significance in addressing grid reliability challenges, particularly in mitigating catastrophic blackouts. By enabling ubiquitous, high-resolution monitoring across distribution networks, this technology directly targets the root cause of historical cascading failures—such as the

2003 Northeast US-Canada blackout—where undetected local faults propagated into system-wide collapses. The applications of PMUs can also be extended to fault detection, system protection, load forecasting, and power flow optimization, among other areas [1].

2. Literature review

2.1 Comparison of PMU and SCADA

With the increasing integration of high-penetration renewable energy and complex load structures into power systems, the limitations of traditional Supervisory Control and Data Acquisition (SCADA) systems in dynamic monitoring and real-time control have become evident. SCADA systems, relying on asynchronous data acquisition with sampling intervals of seconds, provide only scalar measurement [2]and fail to capture the completely dynamic characteristics of transient events such as short-circuit current surges or voltage sags [3]. In contrast, Synchronized Phasor Measurement Units (PMUs), leveraging GPS-based time synchronization with microsecond-level precision, deliver high-resolution (30 – 60 frames per second) synchrophasor data encompassing magnitude, phase, and frequency, significantly enhancing dynamic event detection accuracy.

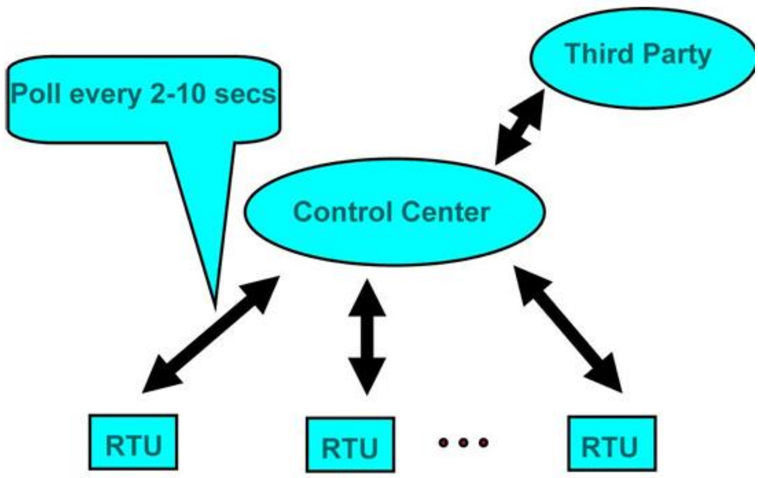

Figure 2.1 The SCADA configuration in which the substation data is gathered at the

control center [4]

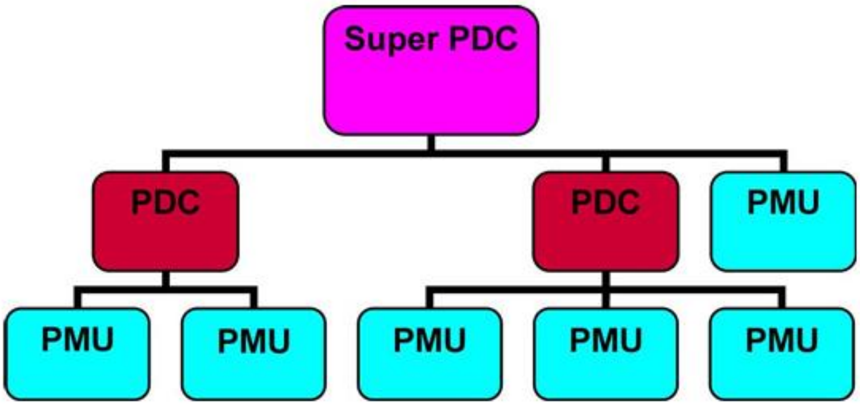

Figure 2.2 The PDCs that collect the data from PMUs [错误!未定义书签。]

Although PMUs offer superior resolution and faster response, their complete replacement of SCADA systems in the short term remains impractical. To bridge this gap, Zhu proposed integrating PMU advantages into traditional power system dynamic estimators. By employing predictive interpolation methods for SCADA measurements, their framework resolves the incompatibility of heterogeneous sampling rates between the two systems [5]. Extensive simulations on the IEEE 14-bus and 30-bus test systems demonstrate that the fused estimator outperforms individual estimators in estimation accuracy. A dynamic variable-weight state estimation framework was proposed by integrating measurements from phasor measurement units(μPMUs) and Supervisory Control and Data Acquisition (SCADA) systems, which significantly enhances the accuracy of real-time state estimation in distribution networks.

Table 2.1 Comparison of supervisory control and data acquisition (SCADA), Phasor Measurement Unit (PMU) and μPMU

ATTRIBUTE	SCADA	PMU&μPMU
Resolution	1 sample every (2-4) sec	(10-120) samples per sec
Observability	Steady state	Dynamic/Transient state
Phase angle measurement	No phase angle	Provides phase angle
Time synchronization	Measurements are not synchronized	Measurements are time-synchronized

Monitoring and control	Local	Wide area & Local

When μPMU is large-scale deployed in distribution network, massive phasor data analysis and storage methods become a difficult problem. The Berik University team developed a real-time network of μPMU and a powerful time series database called the Berik Tree Database (BTrDB). Capable of continuously writing and reading over 16 million points/cluster nodes per second, the database features advanced query capabilities and university storage, supporting novel analysis and visualization techniques [6].

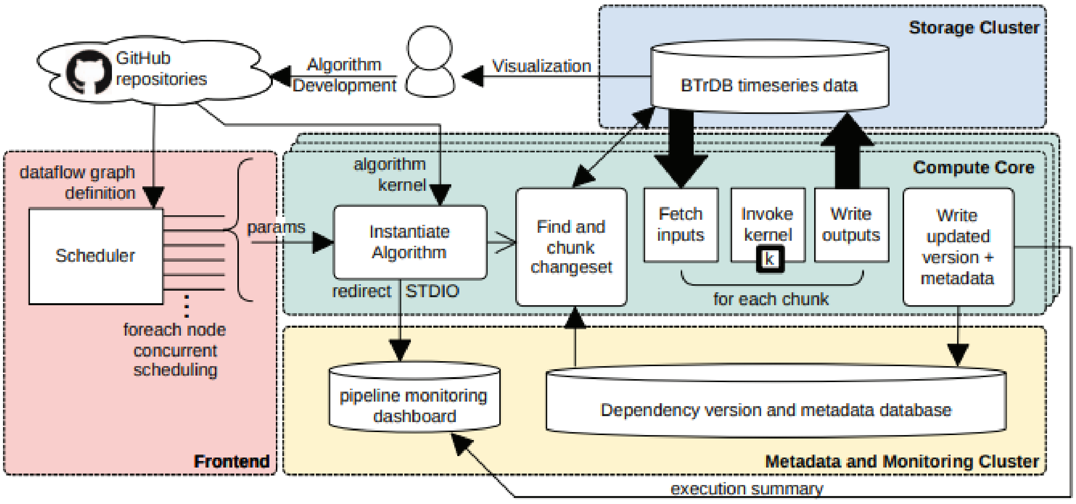

Figure 2.3 The BTrDB framework

The substantial procurement costs of PMUs remain a persistent economic challenge for power utilities. To address this limitation, researchers have proposed optimal PMU placement strategies, which strategically minimize the number of deployed units while maintaining grid observability, thereby significantly reducing the operational expenditures associated with power system health monitoring [7,8].

The strategy of reducing the number of PMUs through optimal placement methodologies fails to fundamentally address the persistent economic challenge posed by the high intrinsic cost of PMU hardware and deployment. The μPMU achieves an order of magnitude cost reduction while ensuring the core measurement accuracy.

2.2 Low-cost Micro-PMU schemes

In recent years, universities and research institutions worldwide have actively engaged in the development of μPMUs. A notable advancement occurred in 2014 with the introduction of the μPMU, a collaborative effort by the University of California (UC), the Electric Power Standards Laboratory (PSL), and Lawrence Berkeley National Laboratory (LBNL). Designed specifically for distribution systems, this device adheres to the IEEE Standard C37.118, which establishes foundational criteria for phasor measurement in power systems. Compared to conventional PMUs deployed in transmission systems, the Micro-PMU achieves a significant cost reduction while maintaining high precision, with a phase angle error of less than 0.01° and a magnitude error below 0.2% [9].

Figure 2.4 Model PQube3 developed the University of Virginia Tech

In 2014, the University of Illinois completed voltage acquisition using the myRIO-1900 acquisition card, time synchronization using GPS, and then sent the data to the open-PDC server for display and archiving. Archived data can be used to validate system models and identify the causes of grid instability. The measurement accuracy of the system meets the requirements of IEEE protocol, and the hardware design cost is about 350 dollars [10].

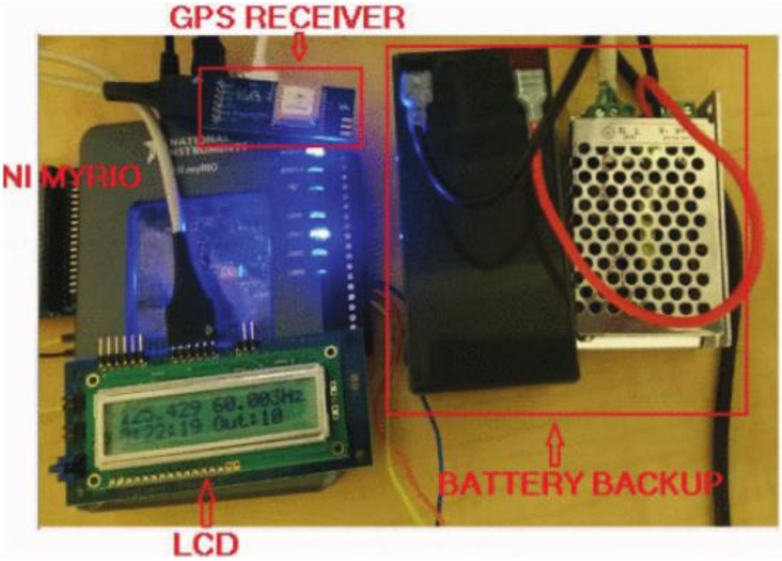

Figure 2.5 μPMU developed by the University of Illinois [10]

In 2017, Thomas Chau developed μPMU utilizing Intel FPGA's Cyclone V SoC hardware and an improved interpolated discrete Fourier transform (i-IpDFT) algorithm for phasor measurement [11]. The study analyzed that the hardware cost of the Cyclone V SoC ranged between 100-200 dollars and the total cost of the μPMU is about 500 dollars. A low-cost scheme is presented [12]. The Raspberry PI hardware board is used as the computing unit, MCC USB201 is used as the data acquisition unit, and the GPS module based on MTK3339 chip is used to provide the UTC time information to the Raspberry PI. The final TVE under steady state conditions is 0.25% of the total hardware cost. It was about 250 euros. Rafael Nilson Rodrigues et al. developed a prototype μPMU using a Digital Signal Processor (DSP) [13]. The study conducted a comparative analysis of several mainstream embedded processing boards available on the market, demonstrating that the STM32F4 series satisfies the minimum computational and real-time processing requirements for μPMU implementation.

Table 2.2 Comparison of price and accuracy

Research institutions	Price	Accuracy	Platform
PSL and BNL	500 dollars	fully certified to lEC 62053-22 Class 0,2S	unknow
the University of Illinois	350 dollars	unknow	Ni myrio

Thomas Chau	500 dollars	0.25%TVE	FPGA
A. Angioni	250 euros	0.25%TVE	Raspberry PI

All the above-mentioned solutions rely on conventional instrument transformers as sensing devices. However, when measuring high-current applications, CTs exhibit significant limitations, including bulky physical dimensions and constrained dynamic range, which hinder their adaptability to compact or high-precision measurement scenarios. Xiaodong Wang harvests energy from the circuit via a high-density inductor-based power module, measures current and voltage waveforms using a PCB-integrated Rogowski coil and a spatial capacitive voltage divider respectively, and achieves voltage and current acquisition through distributed synchronous sampling [14]. The measurement results are shown in Table 2.3, with an accuracy of less than 0.5%

Table 2.3 The test results of current by using Rogowski coil

Primary current, A	Fitting current, A	Error, %
51.1	53.67	0.32
100.2	99.23	0.12
150	149.73	0.03
200.7	200.93	0.03
250.3	248.66	0.21
299.7	297.31	0.30
351.4	353.30	0.24
399.9	399.09	0.10
450.3	450.14	0.02
501.3	501.88	0.07
550.6	549.52	0.13
599.4	601.65	0.28
650.5	652.08	0.20
700.6	699.18	0.18
751.3	750.85	0.06

However, Rogowski coils are incapable of direct current (DC) measurement and require integration with high-performance amplifiers for low-current detection, which significantly increases system costs.

The TMR sensor, as a new type of current measurement technology, has some unique advantages compared with traditional current transformers (CTs) and Rogowski coils [15]. Firstly, the TMR sensor can measure alternating currents containing direct current components, and it has good linear characteristics. The studies in references have shown that the TMR sensor can achieve wide bandwidth and high dynamic range current measurement, and it has broad application prospects in power electronic systems [16].

Table 2.4 A comparison of the advantages and disadvantages of different current sensing technologies

Current sensing technology	Advantage	Disadvantage
CT	High measurement accuracy within the rated current range	Large; High cost;
Rogowski coils	Low weight; Good electrical insulation	Need a high-performance amplifier; High cost;
TMR sensor	High sensitivity and high precision, suitable for both AC and DC	Vulnerable to interference from the external environment

Secondly, the installation and disassembly of the TMR sensor is more convenient, and it also has better long-term stability. Guo and Chen have pointed out that compared with CTs and Rogowski coils, the TMR sensor can be directly integrated onto the printed circuit board without a complex installation process. Moreover, due to the absence of mechanical wear, it can provide more stable measurement performance. This is a significant advantage for power electronic devices that require frequent maintenance [1718].

However, the measurement accuracy of the TMR sensor is vulnerable to the interference of external magnetic fields, and corresponding suppression measures need to be taken. Guo has proposed a method based on magnetic shielding and signal processing, which can effectively suppress the influence of external magnetic fields on the TMR sensor [19]. To further improve the measurement performance, Guo have suggested using a TMR sensor array and combining it with a filtering algorithm for signal processing, which can enhance the measurement accuracy and anti-interference ability [20]. Qi Zhu proposed an integrated solution for non-invasive current measurement in overhead cables, featuring a compact device composed of a Tunneling Magnetoresistance (TMR) differential sensor array, instrumentation amplifiers, a data acquisition board, and a Raspberry Pi-based processing unit. Experimental results demonstrated a measured error of less than 4%, which may be attributed to the inherent electromagnetic interference caused by the physical configuration of the cable [21]. It would be a good idea to use TMR sensing technology to replace the traditional transformers of μPMUs.

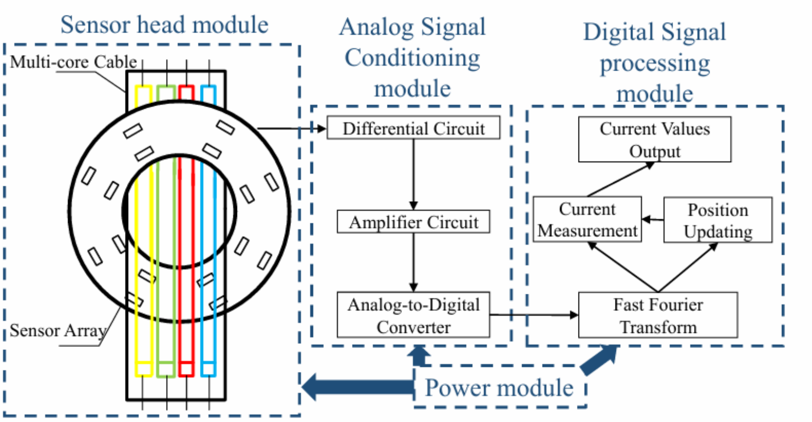

Figure 2.6 Schematic block diagram of the integrated device [错误!未定义书签。].

In contrast, Tunneling Magnetoresistance (TMR) sensing technology offers high sensitivity, high resolution, compact size, and non-invasive measurement capabilities, making it highly suitable for the evolving demands of smart grid applications.

2.3 Phasor measurement algorithm

The development of algorithms for phasor measurement has played a critical role in improving the accuracy and efficiency of PMU systems. Various studies have proposed advanced computational techniques to address challenges such as phase noise, real-time processing, and synchronization errors, laying the foundation for more robust and scalable PMU applications. Among them, the more commonly used methods are zero crossing detection method and Wavelet Transform, least square method, discrete Fourier transform method and other algorithms.

Phasor definition

Phasor representation of sinusoidal signals is commonly used in ac power system analysis. The sinusoidal waveform defined in Equation (1):

$$x(t) = A_1 \cos(\omega t + \phi) \tag{1}$$

where A_1 , ω , and ϕ represent the amplitude, frequency, and initial phase of $x(t)$ respectively. It is commonly represented as the phasor as shown in Equation (2):

$$\begin{aligned} X &= B_1 \mathrm{e}^{\mathrm{j}\phi} \\ &= B_1(\cos\ \phi + \mathrm{j}\sin\ \phi) \\ &= B_\mathrm{r} + \mathrm{j}B_\mathrm{i} \end{aligned} \tag{2}$$

where the magnitude is the root-mean-square (rms) value, B_1=$A_1/\sqrt{2}$, of the waveform, and the subscripts *r* and *i* signify real and imaginary parts of a complex value in rectangular components. The value of ϕ depends on the time scale, particularly where t = 0. It is important to note this phasor is defined for the angular frequency ω; evaluation with other phasors must be done with the same time scale and frequency.

A. Zero Crossing

The zero-crossing detection algorithm is to use the periodicity of the signal to estimate the frequency of the signal by estimating the time interval of the signal passing the zero point. In Fig. 2.14, T_M、T_{M+1}represent the GPS-synchronized 1 Pulse Per Second (PPS) signal and the first zero-crossing instant detected upon the arrival of the PPS signal, respectively. T_n、T_{n+1} indicate the negative-going zero-crossing instants of the signal.

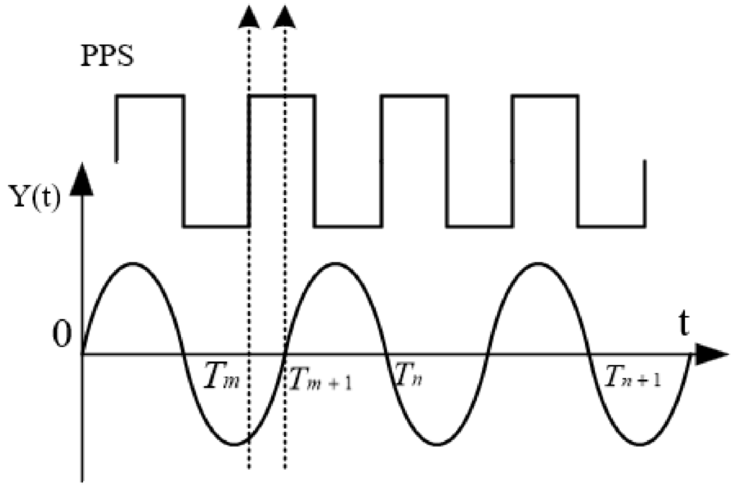

Figure 2.7 The diagram of zero-crossing detection method

The frequency of the measured signal can be estimated by:

$$f = \frac{1}{T_{n+1} - T_n} \tag{2.1}$$

The phase difference between the signal under the test and the synchronization signal is calculated as follows:

$$\theta = 2\pi f (T_{M+1} - T_M) \tag{2.2}$$

The zero-crossing detection method offers advantages of simplicity in implementation and satisfactory real-time performance, as it only requires monitoring sign changes of the signal, resulting in low computational complexity. This makes it particularly suitable for resource-constrained hardware systems. Additionally, it enables rapid tracking of phase variations, rendering it effective for low-frequency signal measurements. However, practical grid signals are often contaminated by harmonics and noise interference, which distort the waveform from an ideal sinusoidal shape and compromise zero-crossing detection accuracy, thereby degrading phasor measurement precision [22]. Furthermore, the method inherently assumes a stable signal frequency, whereas frequency fluctuations—common in real-world power grids—introduce phase estimation errors during frequency deviations.

B. Wavelet Transform

The theory of wavelet transforms was first proposed by French physicist Morlet in 1974. It features variable time-frequency resolution under a fixed window area, with the resolution characteristics following this principle: at low frequencies, it provides high frequency resolution but low time resolution, while at high frequencies, it offers high time resolution but low frequency resolution. This allows localized signal analysis by applying bandpass filters with varying frequency characteristics at different scales.

Let $\phi(t)$ be a mother wavelet. By scaling and translating $\phi(t)$, we define:

$$\phi_{(a,b)}(t) = \frac{1}{\sqrt{2}}\phi(\frac{t-b}{a}) \tag{2.3}$$

where a>0, b∈R. a is the scale factor, b is the translation factor, and $\phi_{(a,b)}(t)$ represents the continuous wavelet basis function derived from the mother wavelet $\phi(t)$. For any signal $y(t) \in L^2(R)$, its continuous wavelet transform is expressed as:

$$\mathrm{WT}_y(a,b) = \frac{1}{\sqrt{a}}\int_{-\infty}^{\infty} y(t)\, \phi^*(\frac{t-a}{b})\mathrm{dt} \tag{2.4}$$

Here, the superscript $*$ denotes the complex conjugate. The mother wavelet is not unique but must satisfy the admissibility condition. Through scaling and translation, the mother wavelet generates a family of basic functions with similar shapes. The wavelet transform essentially quantifies the "similarity" between the analyzed signal and these basis functions.

The performance of wavelet transforms directly depends on the choice of the mother wavelet. Mother wavelets can be categorized into real-valued wavelets and complex-valued wavelets. Real wavelets are limited in applications due to their inability to extract phase information, limited phase-frequency characteristics, and poor matching with target signals. In contrast, complex wavelets are widely adopted because of their rich phase-frequency characteristics and superior compatibility with signal features [23]. The paper proposes a wavelet-based transient detector that identifies transients by analyzing three-level wavelet coefficients of the signal within the sampling window and detecting local maxima. If a transient is detected, the system is deemed to be in a dynamic state, and a dynamic phasor estimation algorithm is selected; otherwise, a steady-state algorithm is used. This approach avoids the complexity of running multiple parallel algorithms.

The innovative EWT - Yoshida method proposed in this paper optimizes the pre -

processing through the WPSD screening mechanism to reduce the computational burden, which is suitable for the sporadic characteristics of sub synchronous oscillations (SSO) [24]. It uses the empirical wavelet transform (EWT) to achieve adaptive signal decomposition, thus solving the problem of selecting traditional wavelet basis functions. It also combines the Yoshida algorithm to perform high - precision parameter estimation in a noisy environment.

C. Taylor series expansion

The Taylor series expansion is a method used for the local approximation of functions. By performing a polynomial expansion near a certain point of a signal, the Taylor series can approximate a signal with nonlinear changes, thus enabling the estimation of dynamic phasors. The application of Taylor series expansion in Phasor Measurement Units (PMUs) mainly focuses on the short-term prediction and trend analysis of signals, and it is particularly suitable for situations where the signal changes are gentle, and the frequency fluctuations are small.

In the application of PMUs, the changes in voltage and current signals may be affected by power grid faults, load variations, or fluctuations of power electronic devices. The Taylor series expansion method can achieve a high-precision estimation of the amplitude and phase of the signal by performing a polynomial expansion of the signal within a relatively short period of time. Specifically, suppose the phasor signal $V(t)$ is expanded into a Taylor series at a certain moment $t0$, which can be expressed as:

$$V(t) = V(t_0) + \frac{dV}{dt}|_{t=t_0}(t - t_0) + \frac{1}{2!}\frac{d^2V}{dt^2}|_{t=t_0}(t - t_0)^2 + \dots. \quad (2.5)$$

$V(t_0)$ represents the initial value of the signal at t_0, $\frac{dV}{dt}|_{t=t_0}$ represents the first derivative of the signal at t_0, and $\frac{d^2V}{dt^2}|_{t=t_0}$ is the second derivative of the signal.

Aiming at the error problem of the traditional Fourier algorithm under dynamic conditions, a four/six-parameter model based on the Taylor-Fourier transform is proposed [25]. By combining frequency tracking technology to compensate for the derivative error of dynamic phasors, the Total Vector Error (TVE) is significantly reduced through post-processing optimization, and real-time and low-latency measurement is achieved in the protection device. However, the computational complexity of the high-order model limits its application in high-order dynamic scenarios.

de la O Serna J A breaks through the traditional assumption of steady-state phasors, puts forward the concept of dynamic phasors and a quadratic Taylor polynomial model [26]. By means of least squares fitting, it estimates the amplitude, phase, as well as the first and second derivatives of the complex envelope. Experiments demonstrate its advantages in high-precision estimation (with the error magnitude reaching the order of 10^-4) and transient detection.

D. Discrete Fourier Transform

The Discrete Fourier Transform (DFT) is pivotal in synchronized phasor measurement, enabling real-time extraction of power frequency parameters from grid signals. While DFT's efficiency and noise suppression—boosted by FFT—make it ideal for embedded systems, asynchronous sampling and the picket fence effect, degrading accuracy. To address these, windowed interpolation FFT combines smooth window function stop suppress leakage with multi-spectral-line interpolation to refine frequency estimates, overcoming resolution limitations. These hybrid methods enhance precision and robustness in noisy or dynamic grid conditions, supporting critical applications like stability analysis, fault detection, and harmonic monitoring.

Definition of DFT

Suppose that $y(t)$ is a continuous periodic signal in the time domain that contains the highest H_{th} harmonic, and the frequency of the h_{th} harmonic is h times the fundamental frequency f_1, where h=0,1,2, ⋯, H. Therefore, the period of $y(t)$ is T=1/ f_1, and $y(t)$ can be expressed as:

$$y(t) = a_0 + \sum_{h=1}^{H} a_h \cos(2\pi f_1 ht) + \sum_{h=1}^{H} b_h \sin(2\pi f_1 ht) \tag{2.6}$$

Where a_0 is the direct current component, and a_h, b_h are the Fourier series coefficients of the h_{th} harmonic, and their expressions are:

$$a_0 = \frac{1}{T}\int_0^T y(t)dt \tag{2.7}$$

$$a_h = \frac{2}{T}\int_0^T y(t)\cos(2\pi f_1 ht)\,dt \tag{2.8}$$

$$b_h = \frac{2}{T}\int_0^T y(t)\sin(2\pi f_1 ht)\,dt \tag{2.9}$$

Assume that the number of sampling points within one fundamental frequency period is N, then we have N=T*f_s. Substitute T=N/f_s, t=n/f_s, and f_1=f_s/N into equations (2.7), (2.8) and (2.9) respectively. Then simplify the above discretized equations, and we can obtain the expression of the discrete Fourier series:

$$a_0 = \frac{1}{N}\sum_{n=0}^{N-1} y(n) \tag{2.10}$$

$$a_h = \frac{2}{N}\sum_{n=0}^{N-1} y(n)\cos\left(\frac{2\pi hn}{N}\right) \tag{2.11}$$

$$b_h = \frac{2}{N}\sum_{n=0}^{N-1} y(n)\sin\left(\frac{2\pi hn}{N}\right) \tag{2.12}$$

By using equations (2.11) and (2.12), the amplitude and initial phase of the h_{th} harmonic can be obtained:

$$A_h = \sqrt{a_h^2 + b_h^2} \tag{2.13}$$

$$\theta_h = \arctan\frac{b_h}{a_h} \tag{2.14}$$

The discrete Fourier transform formula of y(n):

$$Y(k) = \frac{\sqrt{2}}{N}\sum_{n=0}^{N-1} y(n)e^{-j\frac{2\pi kn}{N}} \tag{2.15}$$

k=0,1,2, ⋯, N−1 represents the position of the discrete spectral lines, and the corresponding frequencies are:

$$f_k = kf_s/N$$

For an N-point sequence, performing a Fourier transform requires N^2 computations. To simplify the calculation of the DFT, the periodicity and symmetry of the complex exponential function $W_N = e^{-j2\pi/N}$ can be utilized to reduce computational effort. This method is known as the FFT. The periodicity and symmetry of WN can be expressed as follows:

$$W_N^{(k+N)n} = W_N^{kn} \tag{2.16}$$

$$W_N^{(k+N/2)} = -W_N^{k} \tag{2.17}$$

The sampling frequency f_s of the signal, the signal frequency f_1, and the number of signal sampling points *N* satisfy the following relationship:

$$\frac{N*f_s}{f_1}=\mathrm{M},\ \mathrm{M}=1,\ 2,\ 3,\ \dots \tag{2.18}$$

However, the signal frequencies in the power system are variable, so they do not satisfy the relationship of an integral multiple. In such a situation, spectral leakage and the picket fence effect are likely to occur. The most used technique for suppressing spectral leakage is windowing in the time domain, that is, by changing the window function to suppress spectral leakage.

In the field of phasor calculation, the development of the Interpolated Discrete Fourier Transform (IPDFT) has significantly improved the accuracy and dynamic adaptability of Phasor Measurement Units (PMUs). Traditional DFT suffers from large errors during non - synchronous sampling due to spectral leakage and the picket - fence effect. IPDFT corrects the fundamental frequency estimation through frequency - domain interpolation techniques and combines windowing to suppress sidelobe leakage. Zhang et al. (2023) demonstrated 0.3% TVE improvement with IPDFT in micro-grid applications.

Table 2.5 Comparison of different algorithms

Synchronous phasor measurement algorithm	Characteristics	Disadvantages
Zero Crossing	Simplicity in implementation and satisfactory real-time performance	severe harmonic interference, and other algorithms should be combined for phase measurement
Wavelet	Great dynamic characteristics	High computational

Transform		complexity; Difficult to implement
Taylor series expansion	Improve the phasor measurement accuracy under dynamic conditions, suitable for frequency ramps; low-frequency oscillations.	High computational complexity;
IPDFT	High precision; easy to implement; Low computational complexity.	Select a suitable window function to mitigate spectral leakage.

This table compares different synchronous phasor measurement algorithms. The IPDFT algorithm has the advantages of high precision, easy implementation, and low computational complexity. Its disadvantage is that a suitable window function needs to be selected to mitigate spectral leakage. Compared with other algorithms, the zero - crossing algorithm is simple to implement and has good real - time performance, but it is severely affected by harmonic interference. The wavelet transform algorithm has excellent dynamic characteristics, but it is computationally complex and difficult to implement. The Taylor series expansion algorithm can improve the accuracy of phasor measurement under dynamic conditions, yet it also has a high computational complexity.

Integrating the IPDFT algorithm into the STM32F407 microcontroller offers multiple advantages. In terms of the algorithm's own characteristics, it features high precision, ease of implementation, and low computational complexity. Compared with other algorithms, it has significant advantages in terms of resource consumption and implementation difficulty. Regarding its compatibility with the STM32F407, this microcontroller has limited resources. The low computational complexity of the IPDFT algorithm helps avoid excessive resource consumption and ensures efficient operation within the computing speed range of the microcontroller.

It is worth noting that the computational speed of IPDFT on the STM32F407 is approximately 0.2 ms. This computational delay can be compensated for by group delay.

This means that while ensuring the accuracy of phasor measurement, the delay problem can be effectively addressed, achieving a good balance between real - time performance and accuracy. As a result, the overall performance is stable and reliable, which can well meet the requirements of phasor calculation tasks.

In this study, two-point IPDFT was adopted as the algorithm for calculating phasors, and the formula for calculating phasors is as follows:

For the signal x[n] applies a window function w[n], it's DFT is:

$$X_w[k] = \sum_{n=0}^{N-1} x[n]w[n]e^{-j\frac{2\pi kn}{N}} \tag{2.19}$$

After windowing, the signal spectrum is the convolution of the original spectrum and the spectrum of the window function, and the side-lobe leakage is suppressed. Taking the Hann window as an example, its spectral main lobe is relatively wide but the side lobes decay rapidly. The spectrum of the window function, denoted as W[k] can be expressed as:

$$W[k] = \frac{1}{2}\delta[k] - \frac{1}{4}\delta[k-1] - \frac{1}{4}\delta[k+1] \tag{2.20}$$

Assume that the DFT corresponding to the true frequency of the signal is located at a non-integer point $k_0+\delta$ ($\delta \in [-0.5, 0.5]$) and estimate δ through interpolation. Take the magnitudes of the peak point k_0 and its adjacent points: $|Xw[k_0-1]|$, $|Xw[k_0]|$, and $|Xw[k_0+1]|$. δ can be derived using the following formula:

$$\delta = \frac{|X_w[k_0+1]| - |X_w[k_0-1]|}{2|X_w[k_0]| - |X_w[k_0-1]| - |X_w[k_0+1]|} \tag{2.21}$$

Finally, the fundamental frequency estimate is given by:

$$f_0 = \frac{(k_0+\delta)f_s}{N} \tag{2.22}$$

where f_s denotes the sampling rate and N is the number of samples.

We obtain an estimate of the phasor amplitude and phase as:

$$\hat{A} = \frac{\sqrt{2}|X_w(l)|}{|W(-\hat{\delta})|} \tag{2.23}$$

$$\hat{\phi} = phase\{X_w(l)\} \tag{2.24}$$

Balega et al. investigated the effects of window functions and observation periods on IpDFT performance, proposing the use of Maximum Sidelobe Decay (MSD) windows to significantly reduce Total Vector Error (TVE) in both dynamic and steady-state conditions, while meeting the IEEE C37.118 standard requirements [27]. Derisked et al. developed the iterative IpDFT (i-IpDFT) algorithm, which compensates for spectral interference. This enhancement addresses limitations of traditional IpDFT under dynamic conditions, particularly for M-class applications [28].

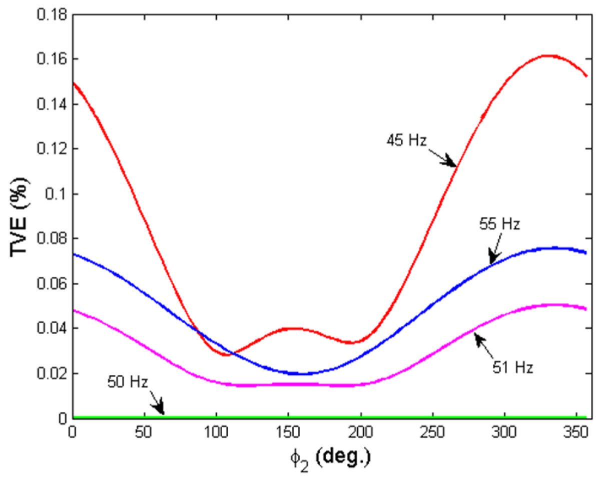

Figure 2.8 IPDFT algorithm test results

The reliability of the IPDFT algorithm is evident in the figure2.4. Within the frequency range of 45 - 55 Hz, the algorithm's performance is well below 1% TVE.

The research results show that during the calculation process of the phasor measurement algorithm, IPDFT has significant advantages, featuring high calculation accuracy and relatively small computational complexity. Compared with some dynamic algorithms, IPDFT is more easily integrated into the processor. This is because complex algorithms will significantly prolong the calculation time, which will undermine the real-time performance of data processing and run counter to the original design intention of the μPMU.

2.4 Application of PMU in power grid

PMU applications are categorized into diagnostic and control applications. Diagnostic applications assist operators and planners in better understanding the current and historical states of distribution systems, thereby providing decision-making support for equipment maintenance, network upgrades, and resource interconnection. Control applications involve real-time directives for specific actions to directly alter the operational state of the network, including circuit topology reconfigurations. Table 1.1 summarizes the application domains of μPMUs in low-voltage distribution networks [29].

Table 2.6 Applications of μPMUs data in distribution networks

Monitoring and Diagnostic Applications	Control Applications
-Event detection	-Volt-VAR optimization
-Fault location	-Adaptive protection
-State estimation	-Distribution network reconfiguration
-Topology status verification	-Microgrid coordination
-Power quality monitoring	
-Phase identification	
-Unmasking loads from net-metered DG	
-Characterization of DER	

Diagnostic application examples

Alireza Shahsavari conducted an experimental analysis based on μPMU data to investigate lightning-induced switchgear system failures in distribution networks [30]. Three Micro-PMUs, installed at distinct locations, were deployed to monitor voltage and current data from different substations and PV power plants. Through these data, the study analyzed voltage transients, reverse power flow, and system responses during lightning events, providing insights into grid behavior under high-impact disturbances.

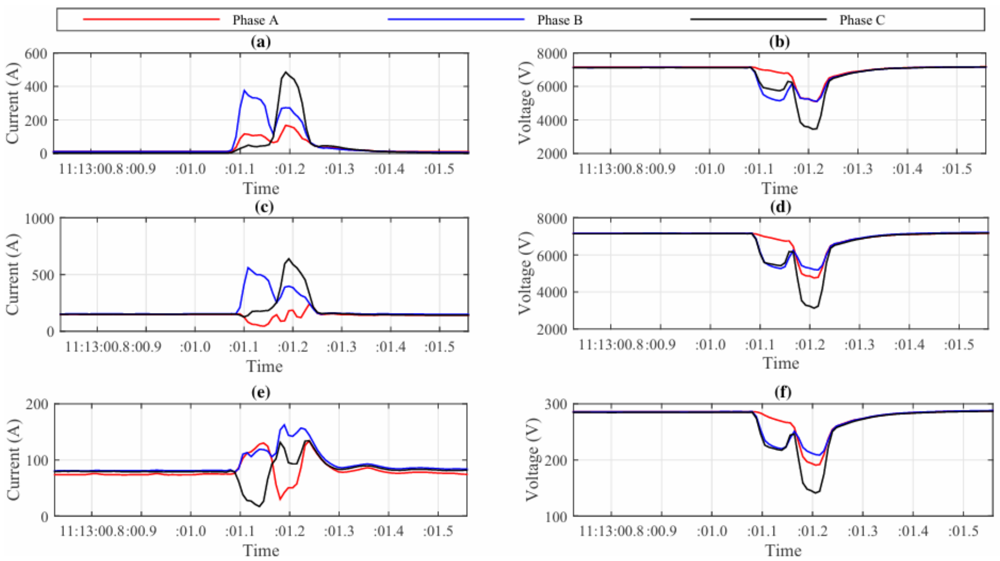

Figure 2.9 Figure 2.9 Three phase voltage and current transients at the first lightening event: (a) and (b) micro-PMU 1; (c) and (d) micro-PMU 2; (e) and (f) micro-PMU 3.

In Figure 2.9 (a) and (b), the current and voltage data captured by Micro-PMU 1 (located near the PV power plant) are presented. During the event, the three-phase currents exhibited substantial transient variations, while the voltages rapidly dropped by approximately 51% to 56% at the onset of the incident. This indicates a transient voltage sag and short-circuit fault triggered by the lightning strike. Figure (c) and (d) display data from Micro-PMU 2 (installed near the substation), revealing similar patterns in current and voltage. The voltage drop magnitude was more pronounced, and the current fluctuations suggest potential reverse power flow phenomena. These observations further confirm that the event was system-wide rather than localized. The consistency across multiple μPMU datasets validates the reliability of μPMU-based monitoring for identifying and analyzing grid operating conditions during fault events.

High-impedance faults (HIFs) typically occur when power conductors meet non-conductive objects such as tree branches or the ground. Characterized by extremely low fault currents, these faults are particularly challenging to detect using conventional methods, such as standard protective devices (e.g., overcurrent relays). Consequently, HIF detection presents a significant challenge for traditional measurement techniques.

Mohammad Ayatollah proposed a novel method for locating HIFs in distribution systems based on synchronized harmonic phasors (specifically the third harmonic component) measured by μPMUs[31]. This approach involves extracting and analyzing the third harmonic components from current and voltage measurements, as these harmonics exhibit distinctive characteristics under HIF conditions. By computing synchronized harmonic phasors and applying impedance-based calculations, the distance between the fault location and the measurement point can be estimated, enabling accurate fault localization.

Accurate fault location helps reduce outage durations and operational costs in distribution networks. μPMU contribute significantly to improving fault location accuracy. Lee proposed a fault location identification algorithm that utilizes pre-fault and post-fault current and voltage phasors recorded by μPMUs. The algorithm demonstrated an absolute mean error of approximately 13.8 meters in simulation environments, equivalent to 0.29% of the feeder length [32].

R introduced a PMU measurement error model for noise characteristic analysis, where noise was intentionally introduced into the system to study its impact on conventional impedance-based fault location method [33]. To analyze noise characteristics, a median filter was employed to extract μPMU noise from raw data. The Monte Carlo method was then applied to generate fault location error samples influenced by μPMU noise. A Gaussian Mixture Model (GMM) was fitted to the observed data, and the goodness-of-fit (GOF) metric from regression analysis theory was used for evaluation. This method was applied to study μPMU noise characteristics and their effect on fault location errors. The study concluded that both μPMU noise and localization errors follow a Gaussian distribution, and the validity of the results was confirmed using actual μPMU measurement data.

S proposed a fault location algorithm utilizing a relatively small number of PMUs. This approach employs a faulted bus location identification index to narrow down the search area, thereby accelerating the localization process [34].

State Estimation (SE) is an important technique used to estimate the states of various devices in a power grid, such as voltage amplitude and phase Angle, as well as other system parameters. SCADA systems often rely on timed or periodic data acquisition, and their measurement accuracy and synchronization are relatively poor. The low frequency of data updates in SCADA systems can lead to delays in state estimation and affect real-time performance, especially when the processing system changes rapidly. In contrast, the data provided by PMU is synchronized in real time, which can capture the dynamic characteristics of the grid in high frequency cases such as short circuit faults, voltage fluctuations, etc., and can simultaneously monitor the phase Angle changes of multiple devices.

Xu proposed a real-time state estimation framework for distribution networks that integrate high-resolution μPMU data with low-resolution smart meter data [35]. The framework divides the distribution network into multiple zones, where micro-PMU measurements are utilized to detect and localize abrupt power variations within each zone. When no abrupt power variations occur, linearized measurement equations are applied to track the state of each zone. In the presence of abrupt power variations, an iterative state estimation process is initiated. This process generates optimized initial values for iterations based on the location and magnitude of power variation, ensuring rapid convergence and high estimation accuracy.

M apply linear state estimation methods for system state estimation of different types of measurements, including μPMU measurements and pseudo-measurements [36]. performance than WLS for certain conditions. Linear DSSE has similar performance to standard nonlinear weighted least squares (WLS) estimates, but under certain conditions, linear DSSE performs better than WLS. The measured values of μPMU and SCADA are used for dynamic variable weight state estimation, which improves the accuracy of real-time state estimation of distribution network [37].

Control application examples

A method for deploying μPMU in the distribution network and improving system integrity protection is proposed by implementing adaptive protection. The method takes uncertainty into account and updates the overcurrent relays in the microgrid according to the changes [38]. The algorithm is based on the impedance estimation obtained by the μPMU installed at the common coupling point to detect the uncertainty. In addition, uncertainty detection of the microgrid is sent by PMUs installed at different locations of the microgrid.

A proper μPMU layout ensures that critical nodes and regions are adequately monitored, improving the system's real-time perception of voltage, current, and phase Angle, especially in dynamic load changes and renewable energy fluctuations. Zhao proposed a hybrid approach based on a global search algorithm to select the optimal location for the full observability of μPMU in the distribution network [39]. The method obtains the optimal solution in a reasonable calculation time. It has three main steps :(i) identifying candidate locations, (ii) searching for the minimum number of μPMU, and (iii) redundant comparisons.

2.5 Research Gaps and Thesis Contribution

Class M PMUs requires 1% TVE at 10 Hz reporting rates, but FPGA-dependent designs dominate compliant implementations-a barrier for COTS-based micro-PMUs. This work prioritizes TVE compliance over reporting rate, targeting 1 Hz updates to accommodate resource-constrained hardware.

The existing research on μPMU has the following key challenges:

1) Trade-off between Hardware Cost and Performance: Although the miniature PMU in the laboratory environment can achieve a TVE (Total Vector Error) of less than 1%, such as 1313, it relies on high-end FPGAs (such as Xilinx Zynq) or custom PCBs, resulting in a single-unit cost of over 500 dollars, making large-scale deployment difficult.

2) Limitations of Sensing Technology: Traditional current transformers (CTs) and Rogowski coils are bulky and expensive, have low measurement resolution, and are unable to measure the DC component. Moreover, the application of TMR technology in μPMU has not been fully verified.

3) Algorithm resource consumption: The real-time performance of complex dynamic phasor algorithms on commercial off-the-shelf (COTS) microcontrollers such as the STM32F4 has not been resolved. At the present stage, relying on cloud computing for

phasor algorithms has increased its burden

This thesis fills the gap through the following innovations:

1) By using commercial off-the-shelf (COTS) components (STM32F407 + AD7606), the hardware cost is reduced to less than 150 dollars.

2) Integrate TMR sensing into the μPMU and evaluate the performance of TMR technology through experiments.

3) Using the Two-point IPDFT algorithm with relatively low computational requirements and integrating it into the processor as the phasor calculation algorithm for this study can significantly reduce the burden of cloud computing.

3. Research Methodology

3.1 System overview

The μPMU designed in this study consists of a signal processing circuit, data acquisition unit, GPS module, control and calculating unit, wireless communication module, and cloud platform. The system architecture is illustrated in the block diagram below.

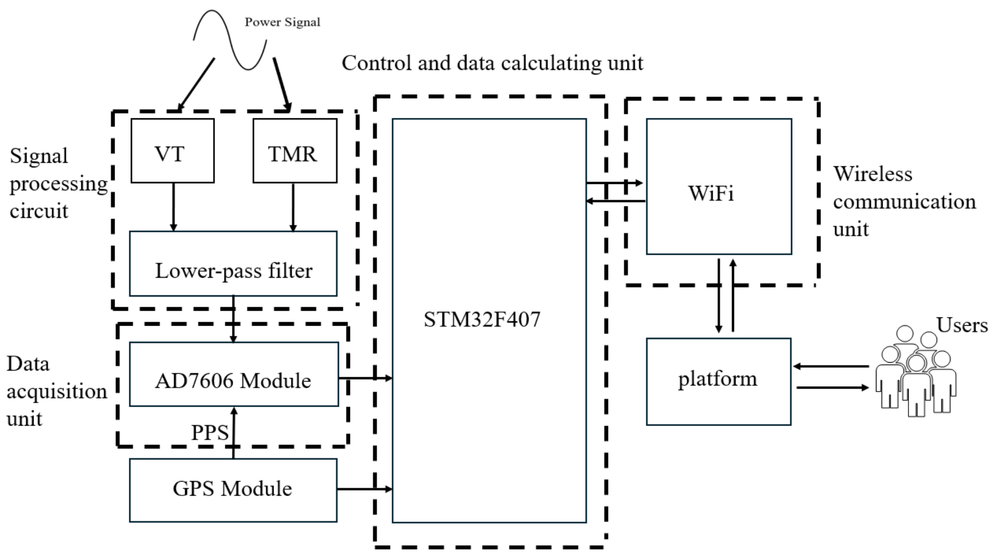

Figure 3.1 System framework of μPMU in this study

Voltage and current signals in the power system are measured using a voltage transformer and Tunnel Magnetoresistance (TMR) sensing technology, respectively.

The voltage transformer steps down the ±220 V AC voltage to a ±5 V AC signal. After passing through front-end conditioning circuits, the signals are filtered by a low-pass filter circuit to suppress high-frequency harmonic interference. The filtered analog signals are then digitized by an analog-to-digital converter (ADC). The AD7606, a 16-bit, 8-channel simultaneous sampling ADC, is selected for this stage, which communicates bidirectionally with the microcontroller unit (MCU) via an SPI interface. The GPS module provides time synchronization for the system and timestamps the data. An STM32F407 microcontroller serves as the control and computation unit, managing the operation of all subsystems, calculating phasor parameters (magnitude, phase, frequency), and transmitting results to the wireless communication module. The wireless unit transmits the processed data to an IoT cloud platform via the MQTT protocol. Users can access real-time grid operational data from the cloud platform through mobile terminals.

This system offers a reliable solution for user-side monitoring of power grid operating conditions, combining high-precision measurements with cloud-based data accessibility.

3.2 Hardware design

3.2.1 Control and calculating unit

STM32F407VGT6 chips are used in the control and computing unit of this system, and the schematic circuit is shown in Figure 3.2. The STM32F407 is a high-performance 32-bit microcontroller based on the ARM® Cortex®-M4 core, widely employed in the design of power system monitoring devices. With a clock speed of up to 168 MHz and an integrated Floating-Point Unit (FPU), it efficiently executes complex power system algorithms, such as Fast Fourier Transform (FFT) harmonic analysis and real-time phasor calculations, meeting the requirements for high-precision data processing.

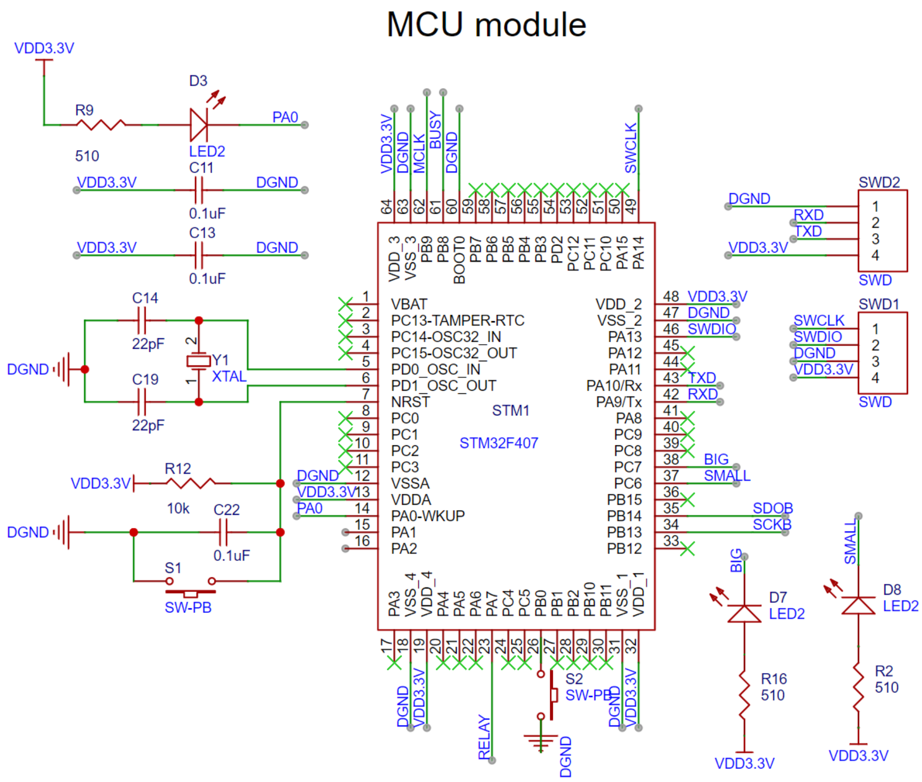

Figure 3.2 The schematic circuit of STM32F407VGT6

Time synchronization capability stands as another core advantage of the STM32F407 in power monitoring applications. Its embedded high-precision Real-Time Clock (RTC) and timers (the 32-bit TIM2) can synchronize with the Pulse Per Second (PPS) signal from a GPS module to achieve microsecond-level time synchronization accuracy. This feature is critical for timestamp generation in μPMUs, ensuring a time error below 1 us, which fully complies with the stringent synchronization requirements of wide-area monitoring in power systems.

For communication and system expansion, the STM32F407 offers diverse interface options. It supports conventional communication protocols such as SPI, I2C, and UART, enabling seamless connectivity with sensors and external storage devices. Additionally, its integrated Ethernet MAC and USB OTG interfaces provide flexibility for wired data transmission. To address wireless communication needs, the microcontroller can be extended with modules supporting LoRa, Wi-Fi, or 4G, adapting to IoT protocols like MQTT and CoAP. This allows real-time transmission of grid data to cloud platforms for remote monitoring and analysis.

3.2.2 Signal processing circuit

A) Voltage transformer

The accuracy of sensor devices directly affects the precision of the PMU. Therefore, high-accuracy sensors must be selected, and their measurement range should exceed the voltage level of the low-voltage distribution network. The system uses HPT-205A voltage transformers as the voltage measuring device. The following table shows the performance of the device.

Table 3.1 The parameters of HPT-205A

Parameter	Values	Unit
Rated Input Current	2	mA
Rated Output Current	2	mA
Maximum Input Curren	10	mA
Maximum Output Curren	10	mA
Rated Point Phase Error	≤5‘ (with compensation)	degree
Accuracy Class	0.1	Class
Frequency Range	0.02-10	kHz
Load Resistance	≤500Ω	Ω

The Table 3.1 demonstrates that the device's voltage measurement range spans 0–660 V, fully accommodating measurements for 220 V systems. Additionally, it supports frequency measurements at 50 Hz. With an accuracy class of 0.1 (corresponding to a measurement error of 0.1%, well below the 1% threshold), the device meets the stringent measurement requirements for μPMU sensors, ensuring high precision and reliability in power system monitoring applications.

The application circuit of the voltage transformer is illustrated in the Figure below

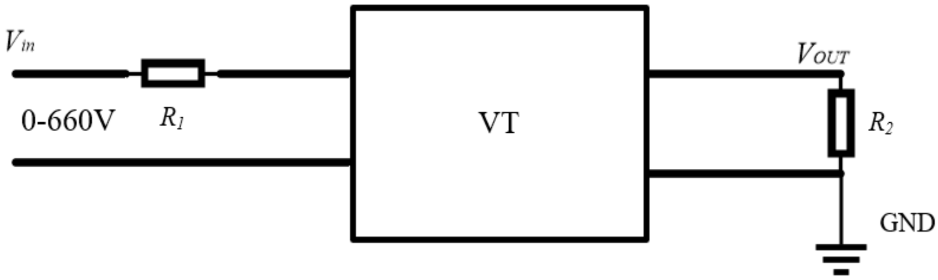

Figure 3.3 The circuit of the voltage transformer

The relationship between the input and output voltages of this circuit can be calculated using the following equation:

$$V_{OUT} = V_{in} * \frac{R_2}{R_1 + R'} \tag{3.1}$$

In the circuit design, R_1 functions as the current-limiting resistor, R_2 serves as the load resistor, and denotes the internal resistance of the voltage transformer (VT). To ensure operational safety and prevent the input current from surpassing the maximum allowable current rating of the VT, R_1 is configured to 100 KΩ. This value is determined based on Ohm's Law ($V=IR$) to restrict the primary-side current flow, thereby avoiding potential core saturation or thermal degradation of the VT.

The internal resistance of the transformer can be ignored compared to 100 KΩ.

$$V_{OUT} = V_{in} * \frac{R_2}{R_1} \tag{3.2}$$

The simplified calculation formula is shown as 3.2. Due to the performance requirements of the device, if the load resistance is greater than 200 Ω, the phase of the output signal will have a serious deviation. To avoid this situation, R_2 is set to 20 Ω. The current output signal amplitude is approximately 0.044 V. To enhance this signal to a measurable range compatible with downstream analog-to-digital converters (ADCs) or data acquisition systems, an amplification circuit with a gain factor of 100 is employed. This amplification process elevates the output voltage to 4.4 V. The schematic of the amplification circuit is shown as follows:

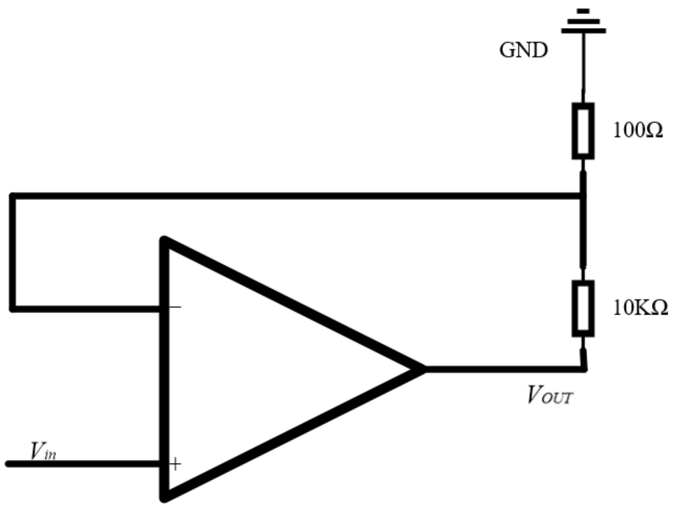

Figure 3.4 The circuit of the amplifier

The calculation formula for gain is as follows:

$$V_{OUT} = V_{in} * \frac{10K}{100} \tag{3.3}$$

To avoid the interference of high-order harmonic noise in the power grid to the signal, a fourth-order Butterworth low-pass filter was designed to make the signal cleaner. The circuit schematic diagram is as follows:

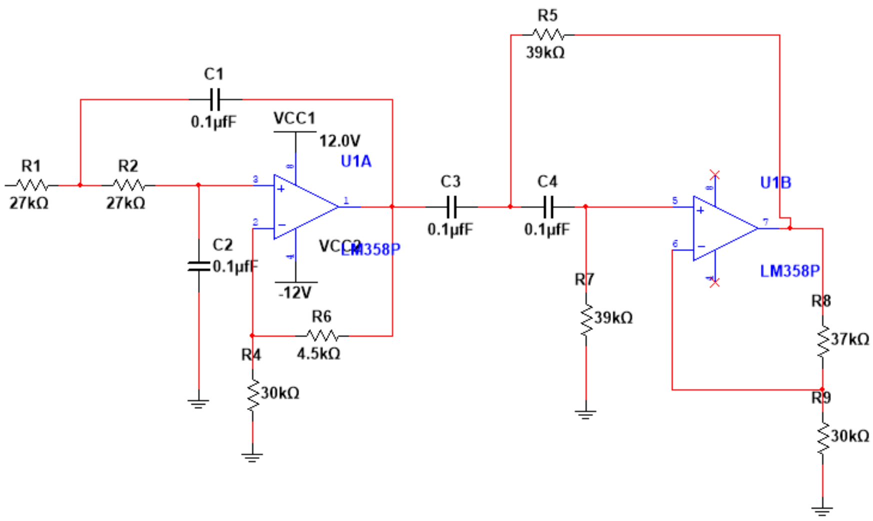

Figure 3.5 The circuit of Butterworth low-pass filter

The cut-off frequency of the circuit signal is approximately 100 Hz. The complete circuit structure designed for voltage measurement is shown in the following Figure

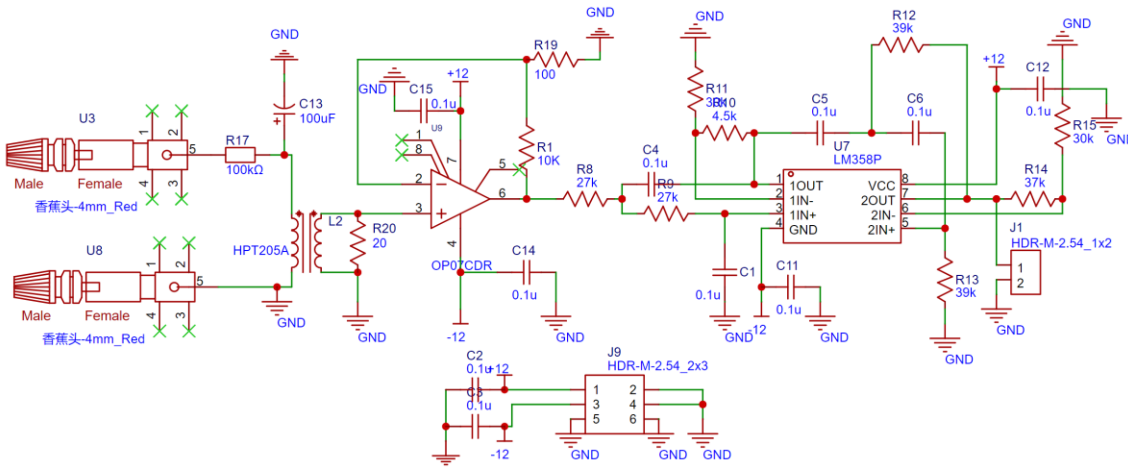

Figure 3.6 Schematic of voltage measurement circuit

B) TMR sensing

In 1995, the Tunnel Magnetoresistance (TMR) effect was independently discovered by Japanese scientist Teru Nobu Miyazaki and German scientist Jürgen Moodera, marking a pivotal advancement in the field of spintronics and magnetic sensing technologies [40].

The Tunnel Magnetoresistance (TMR) effect is a magnetoresistance phenomenon based on the quantum tunneling of electrons, with its core principle rooted in spin-dependent electron tunneling. It typically consists of a sandwich structure (ferromagnetic layer/insulating layer/ferromagnetic layer) forming a Magnetic Tunnel Junction (MTJ). In simpler terms, when electrons pass through an extremely thin insulating layer (the tunnel barrier), their tunneling probability is closely related to the magnetization state of the magnetic materials.

Figure 3.7 illustrates the typical structure and operating principle of an MTJ, which comprises three layers: a free layer, a barrier layer, and a pinned layer. The free layer and pinned layer are both ferromagnetic layers. The magnetization direction of the free layer can change in response to an external magnetic field, while the magnetization of the pinned layer is fixed, usually achieved through an adjacent antiferromagnetic layer that induces the pinning effect. The barrier layer is an ultrathin insulating material, typically on the nanometer scale, which serves as the channel for electron tunneling. Its quality and thickness directly influence the magnitude of the

TMR effect. In Figure 3.7, horizontal arrows represent the magnetization directions of the ferromagnetic layers. Vertical arrows indicate the current flow direction. When the magnetization directions of the two ferromagnetic layers are parallel, the MTJ exhibits low resistance, resulting in a larger current flow. Conversely, when the magnetization directions are antiparallel, the MTJ shows high resistance, leading to a smaller current flow. This resistance switching mechanism enables high-sensitivity magnetic field detection and forms the foundation for TMR sensor applications.

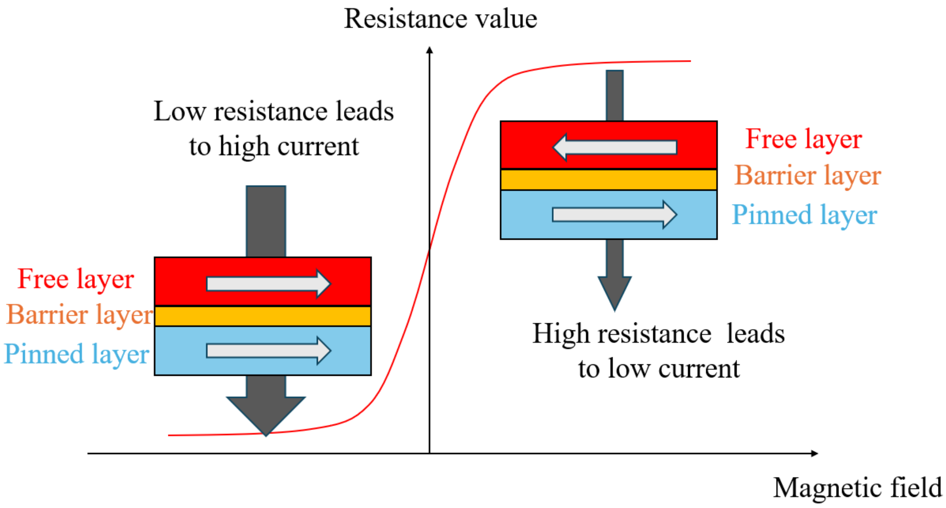

Figure 3.7 The structure of MTJ

In practical design applications, to eliminate the influence of temperature on materials, instead of directly using a single MTJ, a Wheatstone bridge structure composed of four MTJ bridge arms is adopted to design the TMR sensing chip.

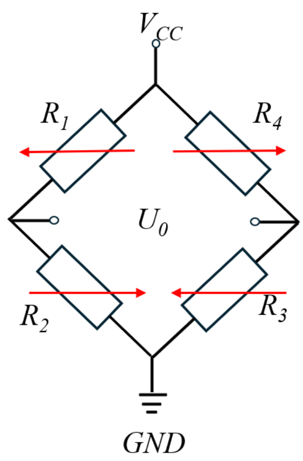

Figure 3.8 The structure of Wheatstone bridge

As shown in Figure3.8, All the resistors have the same resistance value and temperature characteristics. All four bridge arms will change with the external magnetic field. When there is an external magnetic field, the output voltage is $U_0 = \Delta R \cdot V_{CC}/R$, and the sensitivity is V_{CC}.

Currently, among the international companies selling TMR sensing chips is Crocus Technology from the United States. It is one of the earliest companies to research TMR sensing chips and holds a highly authoritative position in the field of magneto resistive chips. In China, Jiangsu Multi-Dimension Technology is a prominent manufacturer of TMR sensing chips. Due to easier accessibility, this paper selects MDT's TMR sensing chips. Several TMR sensing chip products are compared and selected through a review of their data sheets. The performance comparison is presented in Table 3.2 as follows:

Table 3.2 The performance comparison of different TMR chips

Device	TMR2103	TMR2104	TMR2584
Sensitive axis direction	X axis	X axis	Z axis
Supply voltage (V)	0-7	0-7	1-7
Sensitivity (mV/V/mT)	60	31	5
Linearity range (mT)	±3	±8	±10
Linearity	0.5%	1.5%	0.3%
Saturation field	±7.5	±15	±30

The most prominent differences among several chips are in the direction of the sensitive axis, sensitivity, saturation field, linear range, and linearity. By comprehensively considering factors such as the chip assembly method and the chip's sales situation, the TMR2584 was finally chosen. The physical diagram of it is as follows.

Figure 3.9 The physical diagram of TMR2584

A) Design the diagram of current measurement

The current measurement design of the system, based on TMR technology, is shown in Figure 3.10.

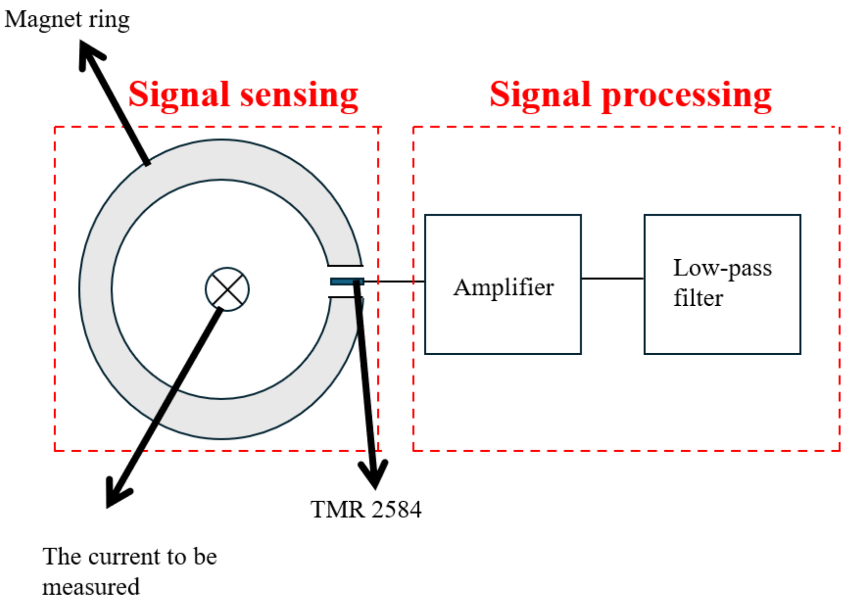

Figure 3.10 The diagram of current measurement

The system employs a magnetic core with an air-gap structure designed to concentrate the magnetic field at the gap region. The core features geometric parameters of 10 cm outer diameter × 1.8 cm inner diameter × 1.8 cm height, with an air-gap width of 1.8 mm. This configuration effectively focuses the magnetic field generated by the current-carrying conductor onto the TMR sensing chip, significantly enhancing field intensity to improve current measurement resolution.

B) Air gap software simulation

This study utilizes Ansys Maxwell 16 for electromagnetic simulation design. The software employs the Finite Element Method (FEM) to accurately model electromagnetic field coupling effects. In this section, we conduct simulations on a fixed magnetic core geometry to establish the correlation between AC current magnitudes and magnetic flux density at the air-gap region. The simulation results are illustrated in Figure 3.11 below.

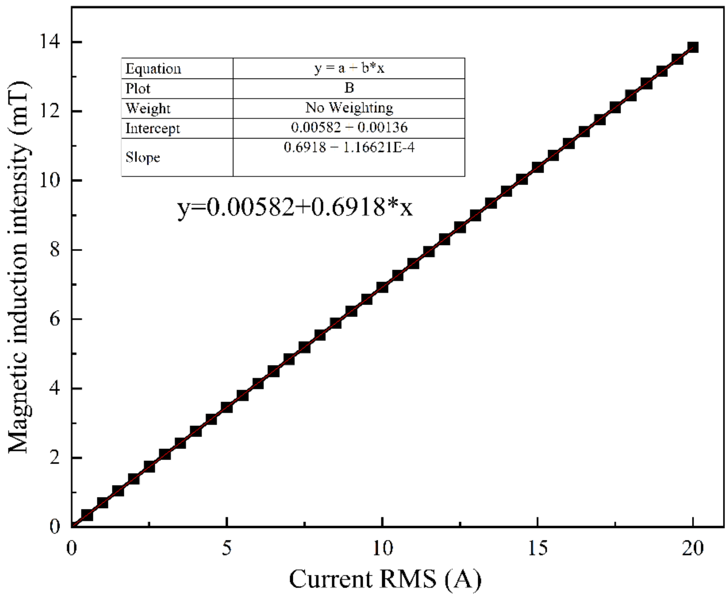

Figure 3.11test results of magnetic induction intensity and current at the air gap

Experimental results demonstrate a significant linear correlation between the magnetic flux density in the air gap and the excitation current. The system maintains excellent linear response characteristics under test conditions where the measured current increases from 0A to 20A with 0.5A increments (fitting curve equation: B = 0.00582 + 0.6918I). This linear behavior validates the feasibility of applying Tunnel Magnetoresistance (TMR) sensors for current measurement in miniaturized Phasor Measurement Units (PMUs), as their wide measurement range (0-20A) fully satisfies the requirements for practical engineering applications. This quantitative relationship provides essential parameters for developing high-accuracy current sensing systems in smart grid and industrial automation applications.

C) Test and calibration of TMR2584 sensor chip

In the designed system, the Tunnel Magnetoresistance (TMR) sensing chip serves as the core detection unit whose critical performance parameters - including linearity, sensitivity, and magnetic hysteresis - directly determine the system's overall metrological characteristics. While the component datasheet provides nominal specifications for these parameters, inherent manufacturing process variations inevitably introduce unit-to-unit deviations. Therefore, comprehensive performance characterization and individual calibration of each TMR sensor are essential prerequisites to ensure measurement consistency and accuracy in practical implementations.

This study employs a custom-developed test platform comprising four principal components: a DC power supply, Helmholtz coil assembly, high-precision gaussmeter, and the Device Under Test (DUT) TMR chip. During the initial experimental phase, calibration of the Helmholtz coil's current-to-magnetic field response characteristics is performed. Specifically, the X-axis coil assembly within the triaxial coil system is selected as the test subject, with magnetic field intensity versus current linearity measurements conducted using a Lake Shore 425® gaussmeter. The experimental procedure comprises the following key steps:

(1) The coil excitation current was programmed in 20mA increments following a cyclic sequence of 0A→+1A→-1A→0A. During testing, the gaussmeter probe's sensing axis was precisely aligned with the magnetic field vector generated by the X-axis coil assembly.

(2) Magnetic flux density variations corresponding to current changes were systematically recorded.

Experimental results presented in Figure 3.12 reveal a strong linear correlation between the magnetic flux density and coil current in the Helmholtz configuration, with a proportionality coefficient of 2.05 mT/A.

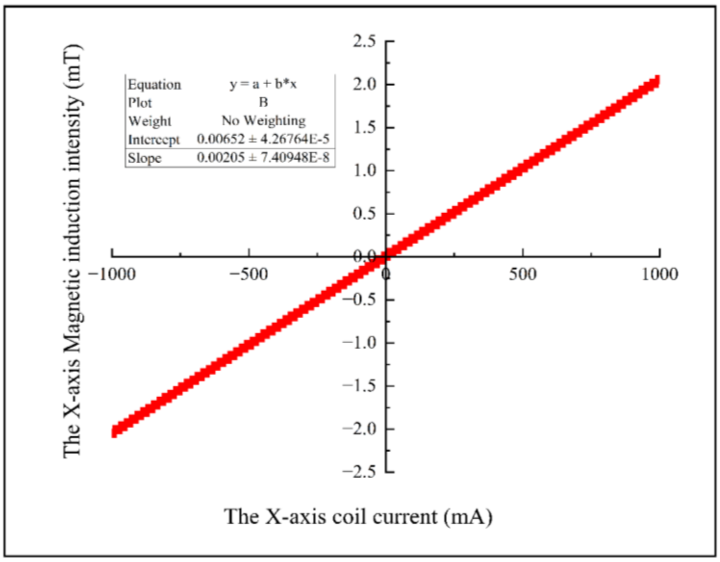

Figure 3.12 The calibration test results of the X-axis of Helmholtz coil

Cross-referencing with the TMR sensor chip's technical datasheet reveals that the TMR2584 device undergoes performance characterization with coil excitation currents spanning ±5.

The system architecture for TMR sensor characterization is schematically illustrated in Figure 3.13. During testing, the TMR chip is first welded onto a dedicated test printed circuit board (PCB). The IT6121B DC power supply independently provides excitation power to both the sensor chip and the X-axis winding of the Helmholtz coil assembly. Concurrently, output signals from the TMR device are acquired and monitored in real-time using a Fluke 287® high-precision multimeter.

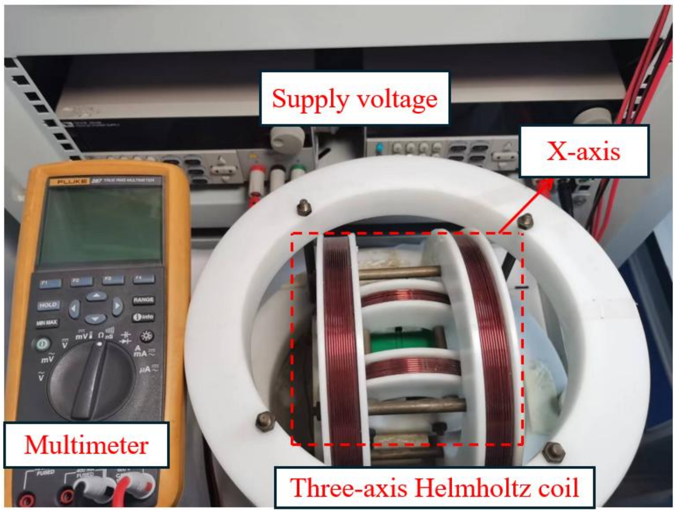

Figure 3.13 TMR sensor chip calibration and testing platform

The TMR sensor operates with the Helmholtz coil current as its input and generates a differential voltage signal as the output. Under fixed supply voltage conditions, the input-output transfer characteristics of the TMR sensor represent the functional correlation between the output voltage and the primary current. Given the specified operating voltage range of 1 V to 7 V in the component datasheet, the device is configured at the maximum rated supply voltage of 5 V DC to optimize signal-to-noise performance. The standardized characterization methodology for the TMR2584 sensor proceeds as follows:

(1) The TMR2584 sensor die is precisely positioned at the geometric centroid of the Helmholtz coil assembly, with its sensing axis meticulously aligned to the magnetic field vector generated by the X-axis winding.

(2) Gradually adjust the input current of the X-axis coil within the range of -5A to +5A at intervals of 500mA.

(3) Collect the output of the TMR2584 chip within the full measurement range Collect the output of the TMR2584 chip within the full measurement range.

The input-output characteristic curve of TMR2584 obtained from the experimental results is shown in Figure 3.14:

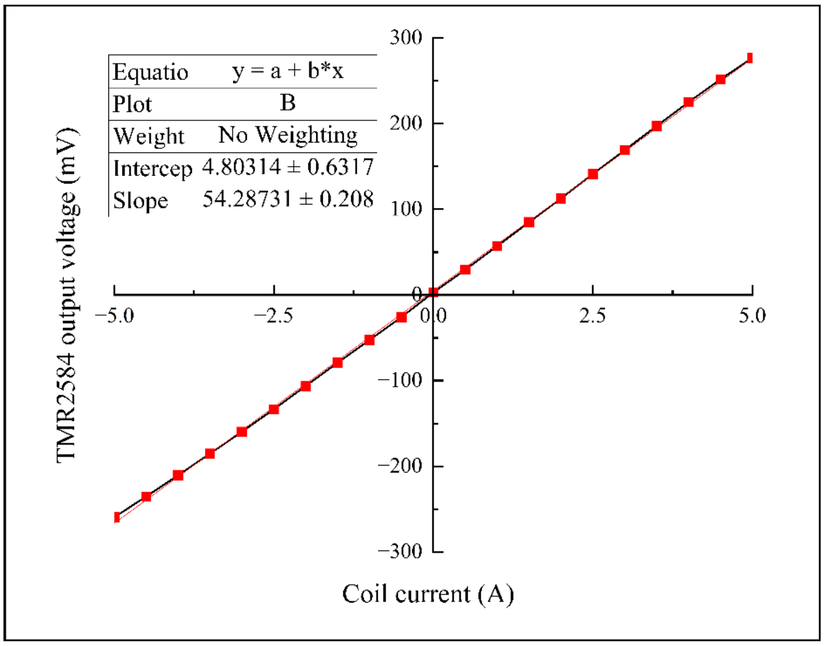

Figure 3.14 Test results of input and output characteristics of TMR2584

The Sensitivity of a magnetoresistance sensor is used to characterize the variation of its output voltage with the magnetic field in a stable operating state. The response characteristic is specifically defined as the ratio of the rate of change of the output voltage to the unit magnetic field intensity. Its definition formula is as follows:

$$S = \frac{\left(\frac{\Delta \mathrm{U_{out}}}{\Delta U_{\mathrm{in}}}\right)}{\Delta H} \tag{3.4}$$

In Equation (3.4), S represents the sensitivity of the sensor. $\Delta \mathrm{U_{out}}$ is the variation of the sensor output. ΔU_{in} is the voltage value of the sensor power supply, ΔH is the variation of the sensor input.

The comprehensive test results demonstrate that the calibrated transfer coefficient of the TMR sensor is determined as 54.28731 mV/A under a 5 V DC supply configuration. Considering the pre-characterized Helmholtz coil current-to-magnetic flux density proportionality coefficient of 2.05 mT/A, the derived sensitivity of the TMR device is calculated as:

$$S = \frac{54.28731\ mV/A}{5\ V \times 2.05\ mT/A} = 5.2963\ mV/V/mT$$

C) Design the TMR2584 current measurement circuit

In response to the matching requirement between the microvolt-level differential signal output by the TMR2584 sensor and the ±5 V input range of the AD7606 analog-to-digital converter, a signal conditioning circuit is designed to achieve an accurate 1000-fold gain amplification and a low-pass filter with a cut-off frequency of approximately 100 Hz. The filter is the same as the voltage part, and the circuit schematic diagram is shown in Figure 3.15.

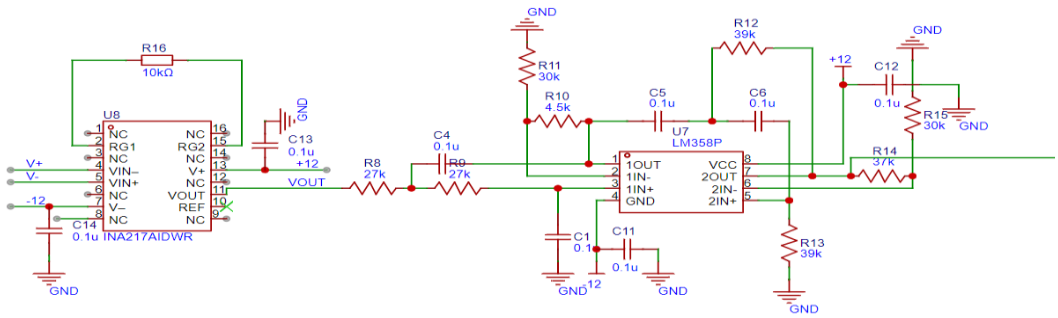

Figure 3.15 Schematic of current measurement circuit

The circuit schematic diagram and PCB of TMR2584 are shown in Figure 3.16. After testing, the gain of the TMR signal processing board is 98.215

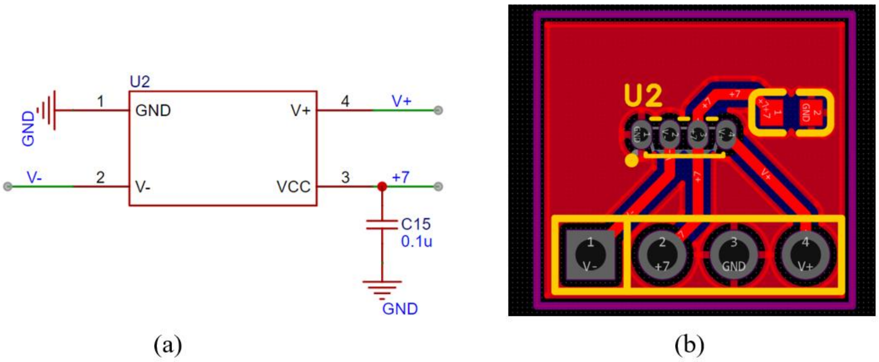

Figure 3.16 (a) is the Schematic of TMR2584 circuit, (b) is PCB about TMR2584

3.2.3 Synchronous data acquisition

To achieve the function of synchronous acquisition, it is necessary to use the GPS module and the analog-to-digital converter in combination. The specific implementation method is to use the PPS (Pulse Per Second) pulse output of the GPS module as the signal for the analog-to-digital converter to start acquisition, and in this way, the data is timestamped.

A. GPS Module

In PMU technology, time synchronization is crucial and is primarily achieved through GPS and the IEEE 1588 network time synchronization protocol. GPS technology, with its high accuracy and reliability, has become the preferred choice for PMU systems. GPS provides sub-millisecond synchronization accuracy through satellite signals, making it suitable for global applications, and it does not require complex local clock management, ensuring high precision and stability.

In contrast, the IEEE 1588 protocol synchronizes clocks through the network. While it avoids reliance on external signals, its synchronization accuracy is typically lower than that of GPS and its implementation is more complex. Although IEEE 1588 can serve as an alternative when GPS signals are unavailable, GPS technology still offers incomparable advantages in PMU systems and remains the most widely used time synchronization technology.

The ATK-S1216F8-BD module, as a high-performance GNSS (Global Navigation

Satellite System) module for high-precision positioning requirements, is designed based on the S1216F8-BD core module of Skytrax. It combines the positioning capabilities of both GPS and Beidou systems and can support 167 parallel channels. Covering the L1 frequency band (1575.42MHz GPS / 1561.098MHz Beidou), with a tracking sensitivity as high as -165 DBM, it can still achieve rapid capture and stable tracking in complex electromagnetic environments. Its core advantages are reflected in multi-system compatibility and high dynamic response: The module supports the output of the NMEA-0183 protocol. The default positioning data refresh rate can reach 20Hz (it can be configured from 1 Hz to 20 Hz through the Skytrax protocol) and is suitable for scenarios with strict requirements for time synchronization accuracy in synchronous phasor measurement (PMU) of power systems (such as microsecond-level time synchronization requirements). In terms of hardware design, the module adopts a compact package (25mm×27mm) and is externally connected to an active antenna through an IPX interface. It supports indoor and outdoor collaborative deployment and is compatible with 3.3V/5V power supply systems, allowing for seamless integration into embedded development platforms (such as the STM32 series).

The module is equipped with a rechargeable backup battery that can store ephemeris data for approximately 30 minutes. It supports a "hot start" function (positioning time <1 second), significantly enhancing the recovery efficiency in the event of a sudden power outage. The output characteristics of its PPS pins can be dynamically configured through software, such as pulse width (1μs to 100ms) and synchronization status indication (constantly on indicates no positioning, flashing indicates successful positioning), providing intuitive feedback for system-level time synchronization. At the software level, the module supports in-depth customization of the Skytrax protocol, including flexible configuration of baud rate (480bps - 921.6kbps), positioning frequency and output data format, and realizes multi-dimensional data extraction of longitude and latitude, altitude, speed and satellite status through the parsing of the NMEA-0183 protocol. In the scenarios of smart grid and distributed energy monitoring, the ATK-S1216F8-BD module provides the underlying time reference for the Wide Area Measurement System (WAMS) through high-precision timestamps and dynamic data refreshing capabilities.

In this system, the module is also connected to the MCU via a UART serial port. The PPS (Pulse Per Second) signal is utilized to trigger an external interrupt on the MCU, thereby controlling the AD7606 to achieve synchronous sampling. The physical appearance and dimensions of the ATK-S1216F8-BD module are illustrated in Figure 3.5. The pin functions of the module and its connection scheme to the MCU are detailed in Table 3.2. The module is powered by a 5V DC supply and communicates bidirectionally with the MCU through the UART2 interface (PA3 as RXD and PA2 as TXD). The PPS pin outputs a high-precision clock pulse, which is received by the MCU via the PF7 pin. This signal triggers an external interruption to synchronize the initiation of AD7606 sampling at precise one-second intervals.

Table 3.3 Pin Functions of ATK-S1216F8-BD and Connection Methods with MCU

ATK-S1218 pins	Function	MCU pins
VCC	Power	VCC
GND	Ground	GND
TXD	Send data	PA3
RXD	Receive data	PA2
PPS	Clock pulse output	PA1

The circuit schematic of ATK-S1216 is as follows:

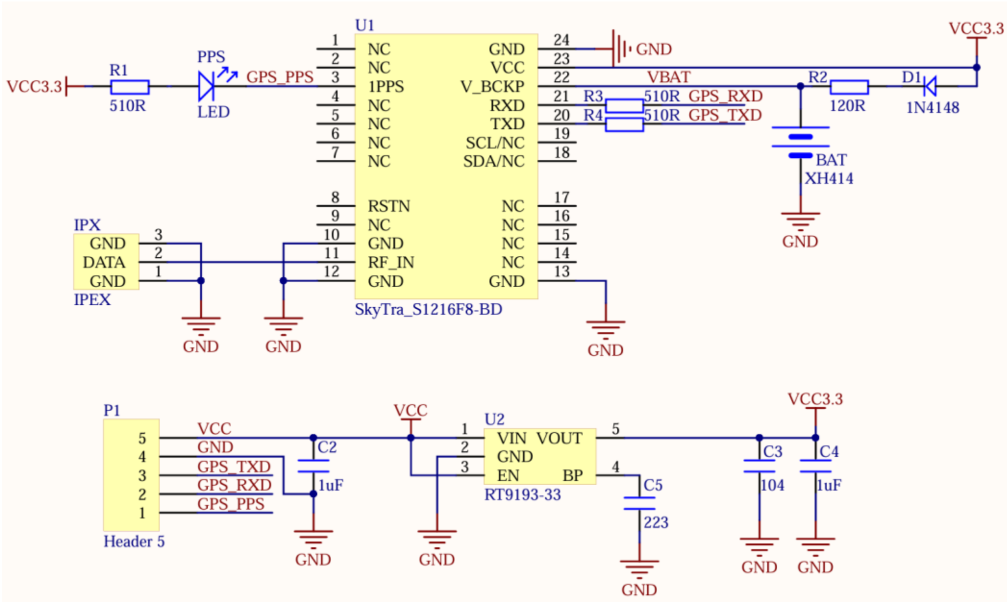

Figure 3.17 The circuit schematic diagram of ATK-S1216

B. Analog-to-Digital Converter

High-precision and stable data acquisition modules are key components that affect the measurement accuracy of PMUs. The AD7606 is a high-performance, multi-channel synchronous sampling data acquisition system (DAS), with its core being a 16-bit bipolar input analog-to-digital converter (ADC), supporting 8-channel, 6-channel or 4-channel synchronous sampling. This device is powered by a single 5V power supply and can handle bipolar analog input signals of ±10V and ±5V. It features a high input impedance of 1MΩ and does not require an external drive amplifier or bipolar power supply, significantly simplifying the system design. Its built-in second-order anti-aliasing filter effectively suppresses high-frequency noise. Meanwhile, it integrates a precise reference voltage source and buffer circuit, ensuring the conversion accuracy and stability. The sampling rate of AD7606 can reach up to 200kSPS (per channel), and it supports flexible digital filter configuration. Through the oversampling function, the signal-to-noise ratio (SNR) can be further enhanced to 95.5dB, and the total harmonic distortion (THD) can be reduced to -107dB, with a dynamic range of 90.5dB. Its low power consumption feature (100 mW in normal mode and 25 mW in standby mode) and 7 kV ESD protection mechanism further enhance the reliability and energy efficiency performance of the system. The AD7606 is compatible with multiple digital interfaces (such as SPI and parallel interfaces),and supports reading data during conversion to optimize throughput efficiency. It is suitable for high-precision synchronous acquisition scenarios such as power line monitoring, multi-phase motor control, industrial instruments, and multi-axis positioning. The circuit schematic diagram of AD7606 is shown as follows:

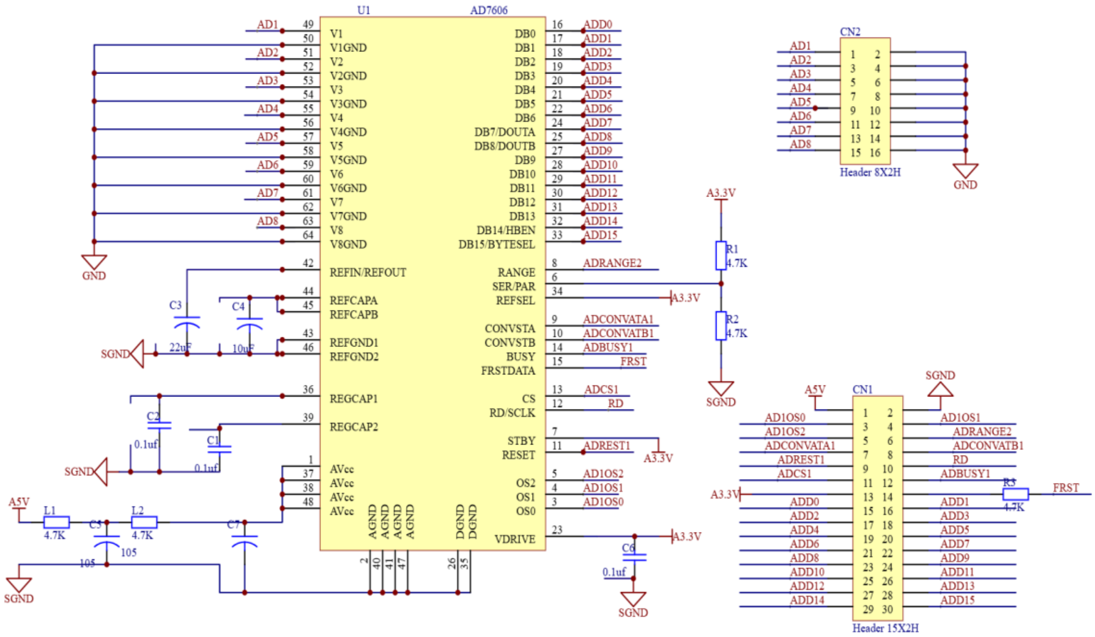

Figure 3.18 The circuit schematic of AD7606

Table 3.4 shows the functions of some important pins of AD7606 and their connection methods with the MCU. The PAR/SER pin is used to select the serial/parallel output mode of the AD7606. In this article, the pull-up resistor is soledR21 selects the serial output mode; The "RANGE" pin is used to select the analog input RANGE. In this system, range sets the pin to zero and set the analog input range to ±5V; The MCU outputs PWM signals through the CONVST_A pin. The number is used to set the sampling rate of AD7606. When the output level of the BUSY pin is high, it indicates the last conversion It has been completed. The rising edge output through the BUSY pin triggers the external part corresponding to the PA15 pin in the MCU Break and read the data of this conversion output from pin DB7 through SPI communication. RD/SCLK is responsible for providing the clock for SPI data transmission.

Table 3.4 Pin Functions of AD7606 and Connection Methods with MCU

AD7606 pins	Function	MCU pins
OS0	Digital filtering	PD8
OS1	Digital filtering	PD9
OS2	Digital filtering	PD10
RANGE	±5V	PD11
REST	Reset	PD13
CONVSTA	Sampling frequency	PD12
CS	enable	PD14
RD	Clock pin	PB13
D7	Data output	PB14
BUSY	Data conversion	PA9

3.2.4 Wireless communication

In this system, it is necessary to send the power grid data from the MCU to the cloud platform for processing, while traditionally. Wired transmission also has problems such as the transmission distance being limited by the line length and the difficulty of wiring in the working environment. This system accomplishes data transmission through wireless communication. Table 3.5 presents a comparison of several relatively common wireless transmission methods at present.

Table 3.5 Comparison of several wireless transmission methods

Characteristics	Bluetooth	Wi-Fi	Zigbee	LoRa
Distance	10m-1.5km	15m-100m	30m-100m	3km-50km
Transmission speed	125kbps-2Mkbps	54Mbps-1.3Gkbps	20kbps-250kbps	0-100bps
Power	low	medium	low	low

It can be seen from the above Table 3.5 that Wi-Fi has the characteristics of high transmission rate and long transmission distance. It can transmit data to any place through Ethernet and meet the requirements of PMU for rapid data upload. Therefore, the system selects Wi-Fi wireless communication technology to achieve data transmission between the MCU and the cloud platform.

The ESP8266 is a highly integrated Wi-Fi System-on-Chip (SoC) designed for IoT applications, featuring exceptional performance and versatile functionalities. The device supports three operational modes: STA (Station), AP (Access Point), and STA+AP hybrid mode. In this system, the ESP8266 is configured in AP mode, where it acts as a wireless hotspot, enabling direct connections from smartphones, computers, and other devices to receive data. In STA mode, the module connects to a wireless network via a router, allowing remote control of devices over the internet. The STA/AP hybrid mode combines both functionalities, enabling simultaneous operation as a network client and an independent access point. This flexibility makes the ESP8266 ideal for applications requiring localized connectivity and internet-based remote management.

In this system, this module is connected to the MCU through the UART serial port, receives the result of the MCU's calculation of phasors and the timestamp information, and sends them to the cloud platform. The circuit schematic diagram of this module is shown as follows

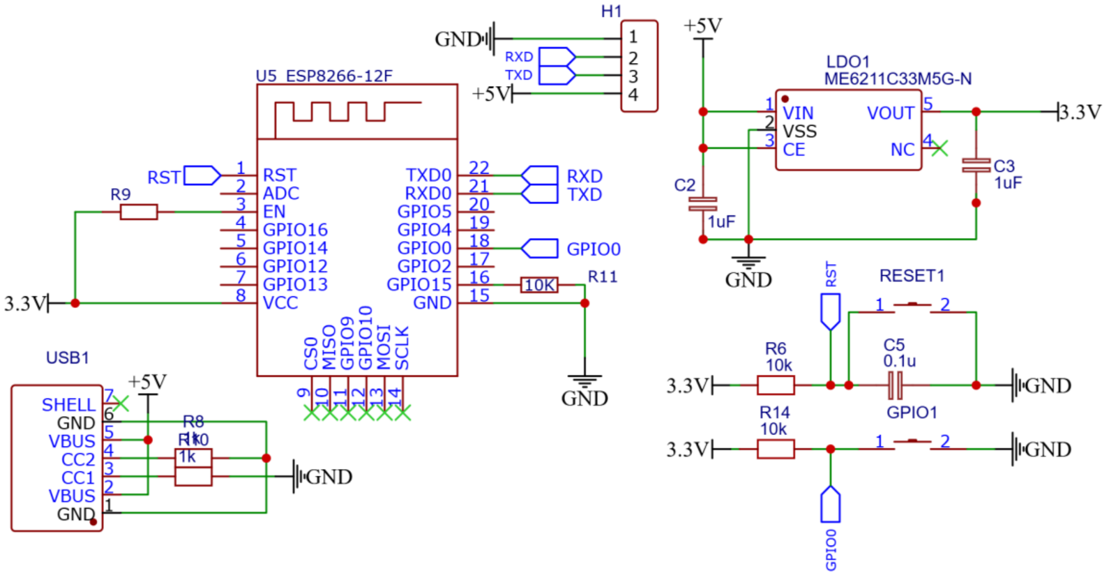

Figure 3.19 The circuit schematic of ESP8266

The pin functions of the ESP8266 module and the connection method between it and the MCU are shown in Table 3.6. The TDX and RDX pins are connected to the PA9 and PA10 pins of the UART in the MCU to complete the bidirectional data transmission. The RST pin can complete the module. The reset function is performed when the PF6 pin is at a low level.

Table 3.6 Pin Functions of ESP8266 and Connection Methods with MCU

ESP8266 pins	Function	MCU pins
VCC	Power	VCC
GND	GND	GND
TDX	Send data	PA10
RDX	Receive data	PA9
REST	Reset	PA5

3.3 Software design

3.3.1 Software system framework

As shown in the Figure, the operational workflow of a GPS time-synchronized data acquisition and transmission system is depicted. The process initiates with system configuration, followed by a validation check for the PPS signal (PPS=1). Upon successful verification, sensor signals are collected and synchronized with GPS timing information to ensure precise timestamp alignment. Phasor quantities (voltage/current phase parameters) are subsequently computed using dedicated algorithms. Finally, the processed data is transmitted via a Wi-Fi module to predefined endpoints.

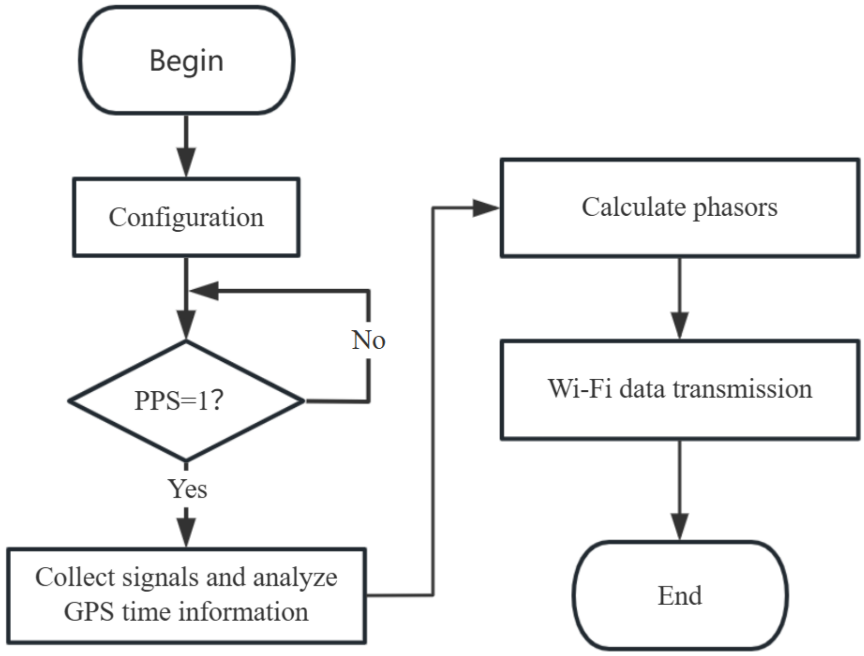

Figure 3.20 Program flow chart in this system

3.3.2 GPS Data Acquisition and Parsing

This system realizes the real - time reception and parsing of NMEA - 0183 protocol data output by the GPS module through the STM32 microcontroller, with a focus on extracting key information such as time, latitude, and longitude. The NMEA - 0183 protocol is a standard communication protocol for GPS devices. Its data frames are organized in ASCII format. A typical frame like GNRMC contains fields such as UTC time, positioning status, latitude, and longitude. The system design takes serial port interrupt driving as the core, combined with buffer management and protocol parsing algorithms to ensure the real - time performance and accuracy of data processing.

The GPS module continuously outputs data through the USART2 serial port at a fixed baud rat. When data arrives, it triggers the USART2_IRQHandler interrupt service routine. The program first detects the start character $, marks the start of a new frame, and resets the buffer index. Then, it stores the data byte-byte into the USART2_RX_BUF buffer. When the newline character \n is detected, it indicates that a frame of data has been completely received. The system sets the flagged flag to notify the main program for parsing. During this process, the program selects the corresponding parsing logic by judging the frame header (such as GNRMC or GPGSV) to ensure compatibility with multiple frame types.

Compared with the processing speed of STM32, the update of GPS/BDS positioning data is relatively slow. Position information is output every second, and even if several data packets are lost, the positioning accuracy will not be affected. This device connects the GPS/BDS module to Serial Port 3 of STM32 and receives the NMEA 0183 protocol data sent by GPS/BDS through the receiving interrupt mode of Serial Port 3.

In the interrupt function of the timer, the highest - order bit of the Serial Port 3 reception flag is set to 1. If the highest - order bit of the Serial Port 3 reception flag is 1, it indicates that the serial port data reception is completed, waiting for the time detection function to process. In the time detection function, the Serial Port 3 reception flag is set to zero, clearing the highest - order bit to prepare for the next reception of GPS/BDS information.

NMEA-0183

In this design, the selected GPS/BDS module is a highly integrated small - scale system. It has a convenient operation mode. Users only need to use AT commands and can complete all tasks through serial communication. Essentially, the core of using this module lies in the parsing of character strings, and this process falls within the category of serial communication programming.

The GPS/BDS module uses the ASCII code format to transmit NMEA - 0183 protocol positioning information. The data frame format of this protocol is as follows:

$aaccc,ddd,ddd,…,ddd*hh(CR)(LF)

'$' serves as the frame command start bit; 'aaccc' is the address field, where aa is the identifier and ccc is the sentence name. The protocol includes various commands such as GNGGA and GNRMC; 'ddd, ddd, ⋯, ddd' are serial port data, which are the key objects for program parsing; '*' is the check - sum prefix; 'hh' is the check - sum, obtained by performing an exclusive - OR operation on the ASCII codes of the characters between "$" and "*" and then converting them into 16 - bit hexadecimal ASCII characters; (CR)(LF) marks the end of the data frame.

In actual engineering projects, $GNRMC (Recommended Minimum Specific GPS/Transit Data) is the most used, with a length of 70 bytes. Most NMEA - 0183 protocol sentences start with a format like this. The output format is fixed, commas always exist, and "*" serves as the end of valid data. Based on these characteristics, by retrieving the positions of commas and extracting information according to the data format, an effective parsing of the NMEA - 0183 protocol can be achieved. The specific implementation code is shown below.

```
if(gt_u8_t.flag_getdata){
        gt_u8_t.flag_getdata = 0;
        memcpy(gt_u8_t.latitude_c, &gt_u8_t.GPS_Buf[20], 10);
        memcpy(gt_u8_t.longitude_c, &gt_u8_t.GPS_Buf[33], 11);
        gt_u8_t.latitude_c[11] = '\0';
        gt_u8_t.longitude_c[12] = '\0';

        temp1 = atof(gt_u8_t.latitude_c);
        temp2 = (uint16_t)(temp1/100);
        temp2 += (temp1 - temp2*100)/60;
        gt_u8_t.latitude = temp2;

        temp1 = atof(gt_u8_t.longitude_c);
        temp2 = (uint16_t)(temp1/100);
        temp2 += (temp1 - temp2*100)/60;
        gt_u8_t.longitude = temp2;

        memcpy(gt_u8_t.time_c, &gt_u8_t.GPS_Buf[7], 2);
        gt_u8_t.time_c[2] = '\0';
        gt_u8_t.hour = atoi(gt_u8_t.time_c);
```

```
        memcpy(gt_u8_t.time_c, &gt_u8_t.GPS_Buf[9], 2);
        gt_u8_t.time_c[2] = '\0';
        gt_u8_t.min = atoi(gt_u8_t.time_c);
        memcpy(gt_u8_t.time_c, &gt_u8_t.GPS_Buf[11], 2);
        gt_u8_t.time_c[2] = '\0';
        gt_u8_t.sec = atoi(gt_u8_t.time_c);
        gps_data.hour = (gt_u8_t.hour + 8)%24;
        gps_data.min = gt_u8_t.min;
        gps_data.sec = gt_u8_t.sec;

        memcpy(gt_u8_t.time_c, &gt_u8_t.GPS_Buf2[11], 2);
        gt_u8_t.time_c[2] = '\0';
        gps_data.num = atoi(gt_u8_t.time_c);

        if(gt_u8_t.longitude > 0 && gt_u8_t.latitude > 0){

            gps_data.latitude = gt_u8_t.latitude;
            gps_data.longitude = gt_u8_t.longitude;
            gps_data.LAT = gt_u8_t.GPS_Buf[31];
            gps_data.LON = gt_u8_t.GPS_Buf[45];
        }
    }
```

3.3.3 External Interrupt-Triggered AD7606 Signal Acquisition

Before starting data acquisition, the program needs to complete the initialization configuration through the AD7606_Init function. First, it calls My_SPI2_Init to set the parameters of the SPI2 peripheral to match the communication timing requirements of the AD7606: the clock polarity (CPOL) is set to low level, the clock phase (CPHA) is set to sample at the first edge, and the baud rate is configured to 10 MHz to maximize the transmission efficiency. Subsequently, the input range is set to ±5 V through the

GPIO control pins, and the oversampling pins OS0 - OS2 are set to low level to turn off the oversampling function, giving priority to ensuring real - time performance. The hardware reset operation is achieved by pulling down the RESET pin and maintaining it for at least 4 clock cycles to ensure that the internal registers of the chip return to their initial states.

After the initialization is completed, the CONVST pin is set to a high level to prepare for the subsequent conversion trigger. Some of the codes are as follows:

AD7606_Init:

```
void AD7606_Init(void){
    My_SPI2_Init();

    AD7606_CS_Set();
    AD7606_RANGE_5V();
    AD7606_OS0_Clr();AD7606_OS1_Clr();AD7606_OS2_Clr();
    AD7606_Reset();
    AD7606_CONVST_Set();
}
```

My_SPI2_Init:

```
    GPIO_InitStruct.Pin = GPIO_PIN_13|GPIO_PIN_15;
    GPIO_InitStruct.Mode = GPIO_MODE_AF_PP;
    GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_HIGH;
    HAL_GPIO_Init(GPIOB, &GPIO_InitStruct);

    GPIO_InitStruct.Pin = GPIO_PIN_14;
    GPIO_InitStruct.Mode = GPIO_MODE_INPUT;
    GPIO_InitStruct.Pull = GPIO_NOPULL;
    HAL_GPIO_Init(GPIOB, &GPIO_InitStruct);
   HAL_GPIO_WritePin(GPIOB, GPIO_PIN_12 | GPIO_PIN_13, GPIO_PIN_SET);
```

To achieve the synchronous acquisition function, when the rising edge of the PPS signal arrives, the flag bit flag_end is set to 1, and the program enters the timer interrupt function. Each time the timer overflow interrupt is triggered, the program calls the AD7606_ReadVol function to perform the data reading operation. This function first pulls down the CS chip - select signal to enable the SPI interface of the AD7606 and then receives 2 bytes of raw data through HAL_SPI_Receive. Since the output of the AD7606 is in two's complement format, the 16 - bit data is reorganized into a signed integer, and is converted into the actual voltage value

After the conversion is completed, the AD7606_StartConv function is immediately called to generate a CONVST start pulse: the level of the CONVST pin is quickly switched, and a new round of conversion is triggered by its falling edge. This design achieves precise control of the sampling interval through the cooperation of the hardware timer and software triggering, with a time jitter of less than 100 ns.

3.3.4 IPDFT Algorithm test

MATLAB is a scientific computing and simulation software with extremely powerful functions, demonstrating unparalleled advantages in the field of algorithm performance verification. The operation interface is shown in Figure 3.21. It has a vast and professional library of functions, which can not only quickly generate power test signals conforming to IEEE standards but also support the construction of various complex signal models. The built-in visualization tools, such as drawing waveform diagrams and spectrograms, can intuitively present the signal changes before and after the algorithm processing, facilitating result analysis. In terms of numerical computation, MATLAB has highly efficient matrix operation capabilities, enabling it to process massive amounts of data rapidly and significantly improving the verification efficiency. Its powerful programming functions allow users to customize algorithm modules, seamlessly connect with mainstream algorithm frameworks, and achieve rapid iteration and optimization of algorithms. In addition, MATLAB also supports interaction with a variety of hardware devices, making it convenient to carry out algorithm verification in real-world scenarios, providing a one-stop solution for the comprehensive evaluation of algorithm performance.

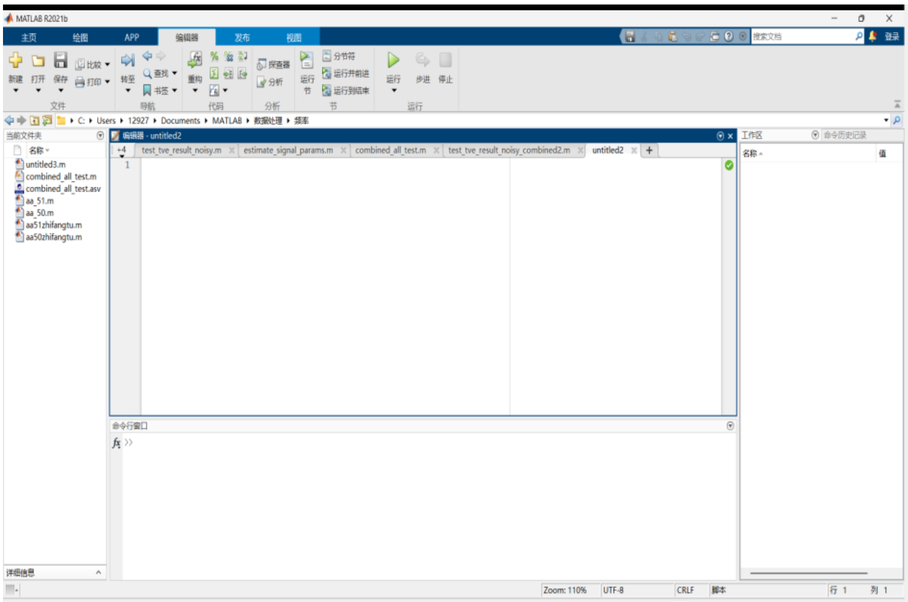

Figure 3.21 The operation interface of MATLAB

This research conducts a comparative analysis of the classical Discrete Fourier Transform (DFT) algorithm and the Improved-Polynomial Discrete Fourier Transform (IPDFT) algorithm using the MATLAB simulation platform. As shown in Table 3.7, at a frequency of 49.5 Hz, the IPDFT algorithm exhibits significantly better performance in key metrics compared to the traditional DFT method.

Table 3.7 Compare of DFT and IPDFT

Algorithm	Frequency Error (Hz)	TVE
DFT	0.5	8.7%
IPDFT	0.031761	0.01635%

The specific implementation steps for calculating frequency, amplitude, and phase using the IPDFT algorithm are detailed in Equations 2.22 to 2.24.

In the dynamic signal analysis of the μPMU, the frequency estimation method based on the Interpolated Discrete Fourier Transform (IPDFT) faces a fundamental contradiction: the trade-off relationship between the time span of the sampling window and the computational performance. From the perspective of signal processing theory, extending the sampling period (increasing the value of N) can improve the measurement accuracy through the following mechanisms:

$$\Delta f=fs/N \tag{3.2}$$

The frequency resolution (Δf) is inversely proportional to N, and a smaller quantization interval is conducive to accurately capturing the frequency offset.

However, this gain in accuracy comes with a significant cost in terms of real-time performance. Table 3.8 presents the results of the Total Vector Error (TVE) and calculation time obtained through MATLAB simulation when the IPDFT algorithm is applied to process the ideal 50Hz signal. An analysis of the data reveals that as the sampling number M gradually increases (corresponding to the number of signal cycles being 1, 2, 3, and 4 in sequence), the TVE value shows a decreasing trend, while the calculation time correspondingly extends. Based on a comprehensive consideration of measurement accuracy and computational resource occupancy, this system finally selects 400 sampling points (corresponding to 2 signal cycles) as the input of signal data for phasor calculation, to achieve a balance between performance and efficiency.

Table 3.8 Performance comparison under different sampling numbers

M	TVE	computation time
200	0.75535%	0.182s
400	0.09418%	0.251s
600	0.02945%	0.335s
800	0.02118%	0.491s

To comprehensively evaluate the performance of the improved Interpolated Discrete Fourier Transform (IPDFT) algorithm in power signal measurement, this study constructs a standardized testing framework on the MATLAB platform to simulate the signal characteristics under the complex operating conditions of an actual power system. The design of the test signals strictly complies with the dynamic test requirements of the IEEE C37.118 standard for the Phasor Measurement Unit (PMU). By synthesizing the fundamental wave, noise, and harmonic components, two typical test scenarios are created: a pure sinusoidal signal (Ideal signal) and an interference signal containing a second - order harmonic and Gaussian noise with a 50 - dB signal - to - noise ratio (SNR) (With 2nd Harmonic Noisy).The fundamental frequency ranges from 48 Hz to 52 Hz (corresponding to a normalized frequency of 0.96 to 1.04, with 50 Hz as the reference). The amplitude is fixed at 1.0 per unit, and the initial phase is randomly distributed within the range of 0 to 2π to eliminate the potential impact of phase alignment on the measurement results. The harmonic component is a second - order harmonic (100 Hz) with an amplitude of 20% of the fundamental wave, which simulates the typical distortion characteristics caused by the nonlinear loads in the power grid. Gaussian noise is generated by setting the SNR to 50 dB to simulate the quantization error of sensors and channel interference. All signals are generated at a sampling rate of 10 kHz, with a data length of 400. A second - order Hanning window is used to suppress the spectral leakage effect, ensuring the accuracy of the time - frequency domain conversion.

During the testing process, the performance of the IPDFT algorithm is quantitatively evaluated through the Total Vector Error (TVE). The TVE is defined as the normalized Euclidean distance between the theoretical phasor and the estimated phasor, and its calculation formula is:

$$\mathrm{TVE}=\sqrt{\frac{(X_r-X_{r0})^2+(X_i-X_{i0})^2}{X_{r0}^2+X_{i0}^2}}\times 100\% \tag{3.3}$$

Among them, X_{r0} and X_{i0} are the real and imaginary parts of the theoretical value respectively, and X_r and X_i are the estimated values of the algorithm.

To fully investigate the robustness of the algorithm against frequency offsets and phase changes, 100 groups of signals with different initial phases are randomly generated at each test frequency point (48 Hz, 48.5 Hz, …, 52 Hz). The maximum TVE value of each group of signals is recorded. Finally, the maximum TVE at each frequency point is used as the evaluation index to reflect the performance boundary of the algorithm under the worst - case operating conditions.

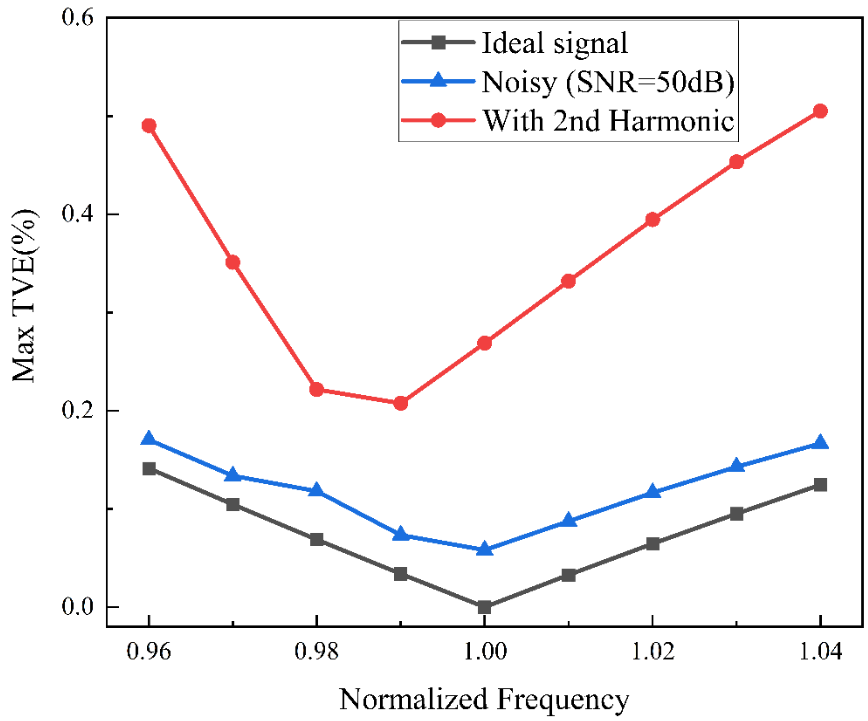

Figure 3.22 The test results of IPDFT algorithm

The test results show that the IPDFT algorithm exhibits excellent measurement accuracy and anti - interference ability under different frequency offset conditions. As shown in Figure 3.22, the maximum Total Vector Error (TVE) of the ideal signal (without noise and harmonics) is approximately 0.1%, which is significantly better than the 1% limit requirement of the IEEE standard for protection - class PMUs. In the interference scenario with a second - order harmonic and Gaussian noise, the maximum TVE rises to 0.5%, still meeting the standard's requirements for measurement accuracy.

Further analysis of the frequency - error distribution characteristics reveals that the TVE reaches its minimum value near the nominal frequency of 50 Hz (normalized frequency of 1.0) (TVE < 0.05% for the ideal signal) and shows a non - linear growth trend with frequency offset. For example, at 48 Hz (normalized frequency of 0.96) and 52 Hz (normalized frequency of 1.04), the TVE rises to 0.5% and 0.6% respectively, which is consistent with the theoretical response characteristics of the algorithm's spectral interpolation kernel function. This phenomenon indicates that the algorithm's dynamic tracking ability for the fundamental frequency remains stable within a ±2 Hz frequency offset range.

3.3.5 Wireless Communication data transform

To ensure interoperability and efficient transmission, raw data from the μPMU—including voltage magnitude, frequency, GPS timestamps, and device status—are formatted into a structured payload. Key codes include:

```
sprintf((char*)data,"AT+MQTTPUB=0,\"$oc/devices/dong_service/sys/propertie
s/report\","""\"{\\\"services\\\":[{\\\"service_id\\\":\\\"dong_service\\\"\\,\\\"properties\\\
":{\\\"FRE\\\": %.7f\\,\\\"SCOPE\\\": %.7f\\,\\\"PHASE\\\": %.7f\\}}]}\",0,0\r\n",
my_fre, my_scope, my_phase);
```

The ESP8266 Wi-Fi module is configured to operate in Station (STA) mode, connecting to a local router for internet access. Data transmission follows the MQTT protocol, chosen for its low bandwidth consumption and support for asynchronous communication. Key codes include:

```
while(!Esp8266_SendCmd("AT+CWJAP=\"dongyazz\",\"xiaozhou20010825\"\r\n",
20)){}
while(!Esp8266_SendCmd("AT+MQTTUSERCFG=0,1,\"NULL\",\"67d54ce4aa
00d157701a2848_pmu_data_0_1_2025031510\",\"d310782c0379ffb4f7c0173d6966b
78c9f8c4ecdc45bbce890fa05288b8bdbf0\",0,0,\"\"", 20)){}
while(!Esp8266_SendCmd("AT+MQTTCLIENTID=0,\"67d54ce4aa00d157701a
2848_pmu_data_0_1_2025031510\"\r\n", 20)){}
```

3.2.6 Cloud platform

The cloud platform in this study is built on Huawei Cloud, leveraging its infrastructure to establish three core physical models for data storage, synchronization, and basic processing. As shown in Figure3.23

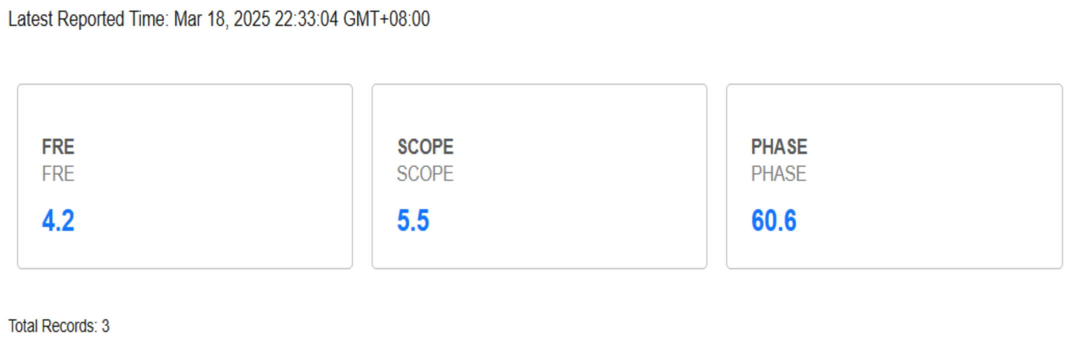

Figure 3.23 Three core physical models for data storage

The data upload workflow is initiated by the μPMU's wireless module, which transmits JSON-formatted measurements to a RESTful API endpoint hosted on Huawei Cloud. Each payload is authenticated using token-based security, and successful uploads trigger a confirmation response to the device.

To further enhance the platform's capabilities, a visualization module will be seamlessly integrated, leveraging Huawei Cloud's Data Visualization Service (DLI) to create real-time interactive dashboards. These dashboards will dynamically present critical metrics such as voltage amplitude trends and frequency fluctuations, enabling real-time monitoring of signal characteristics with millisecond-level precision. Additionally, geospatial visualization features will be incorporated to map the geographical distribution of measurement devices, facilitating comprehensive spatial-temporal analysis of AC signal data across diverse deployment scenarios.

4. Results and Discussion

In this chapter, tests and experiments on the synchronous phasor system are carried out. First, the modules in the system are tested to ensure the system functions properly. Then, a signal generator is used as the signal source for testing to verify the accuracy of the voltage amplitude and frequency measurements of this system. By comparing the measurement results with those of a high - precision digital multimeter, the accuracy of this system in actual measurements is verified.

4.1 Hardware function testing

To ensure the normal operation of the PPS triggering function of the time synchronization unit ATK-S1216F8-BD, it is necessary to verify its satellite time service performance. The test process is as follows: First, install the USB-to-TTL module driver on the computer side, and establish a serial communication link between the device and the host computer through this module. Subsequently, the GNSS receiving antenna is deployed in an open outdoor area to ensure the strength of the satellite signal. Configure the corresponding serial port parameters (default baud rate is 115200) in the GNSS Viewer software and establish a connection. After the device completes the ephemeris parsing, the real-time returned data includes Coordinated Universal Time (UTC), the number of visible satellites, and geographical coordinate information.， as shown in the Figure

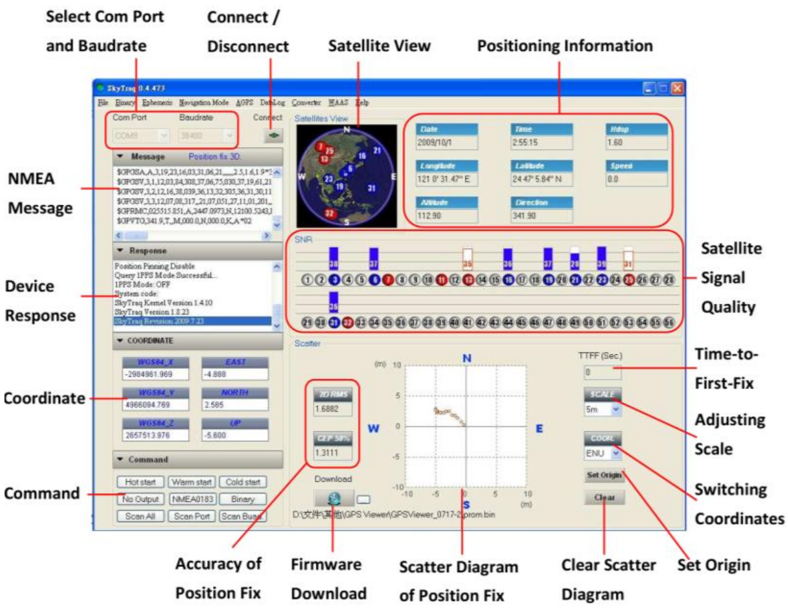

Figure 4.1 The interface of GNSS software

If the location information and the number of satellites is displayed on the software, it indicates that the ATK-S1216 has locked the satellite signal.

In addition, when the time synchronization unit fails to successfully receive the satellite signal, the LED on the unit remains constantly on. After a successful reception, the LED switches to a blinking state with a blinking period of one second. By observing the state of the LED, it is possible to quickly determine whether the unit has successfully detected the satellite signal. This, in turn, allows for a further determination of whether the synchronous phasor measurement system has successfully completed the time synchronization.

Next, a Wi-Fi communication test needs to be carried out. First, the ESP8266 module needs to be connected to the USB-TTL converter. Ensure that the 3.3V power supply and the ground wire are correctly connected. At the same time, connect the RXD and TXD to the TXD and RXD pins of the module respectively. Insert the USB-TTL converter into the USB port of the computer, open the Device Manager, and confirm that the device has been correctly recognized. Use AT commands for debugging. Open the serial port debugging assistant and select the correct COM port and baud rate. Enter "AT" in the text box and send it. If the "OK" string is received, it indicates that the module is working properly.

4.2 Data synchronous acquisition testing

Limited by the testing conditions of the laboratory, the amplitude and frequency of the voltage are measured. The measurement results of the Mirco-PMU are compared with those of a digital multimeter to evaluate the system accuracy of the Mirco-PMU.

As shown in Figure 4.2. This experiment employs a signal generator as a reference voltage source to establish a test system. During the testing procedure, both the signal generator and the μPMU utilize active antennas to collaboratively receive satellite signals from the GPS/BDS navigation systems, achieving high-precision temporal synchronization through demodulated PPS (Pulse Per Second) signals. The signal generator is configured in an externally triggered high-level pulse mode, where the arrival of the PPS rising edge automatically initiates the generation of standard test signals while synchronously triggering measurement operations on both the digital multimeter and μPMU. The measurement data is recorded in real-time using Keysight PathWave BenchVue Digital Multimeter data acquisition software developed by Keysight Corporation, whose integrated UTC timestamp functionality ensures temporal reference consistency across all data channels. During post-processing, a temporal interpolation algorithm is applied to precisely align the temporal domains of measurement results from the μPMU and digital multimeter. Through comparative analysis of amplitude discrepancies and frequency discrepancies between the two signal channels, the system's accuracies are ultimately determined.

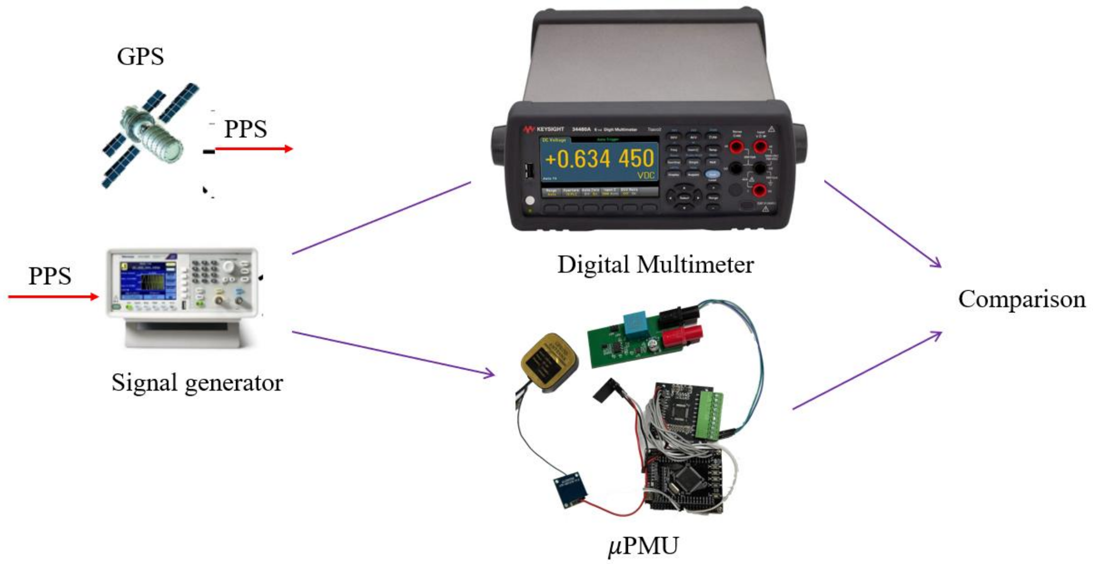

Figure 4.2 System test diagram

The digital multimeter employed in this work is the Agilent 34410A/11A 6½ model, which exhibits exceptional precision in measuring the amplitude and frequency of alternating current signals. Leveraging true root-mean-square (RMS) measurement technology, it supports accurate amplitude quantification at 50 Hz, achieving a measurement accuracy of ± (0.02% of reading + 0.02% of range) for AC voltage amplitude under this frequency condition. For frequency measurement, the instrument demonstrates a high-level precision of 0.005% of the reading, ensuring reliable characterization of signal frequency parameters across its operational spectrum. These stringent accuracy specifications establish its suitability as a reference standard for precise AC signal analysis in scientific and engineering applications.

4.2.1 The test of voltage

A. Frequency Test

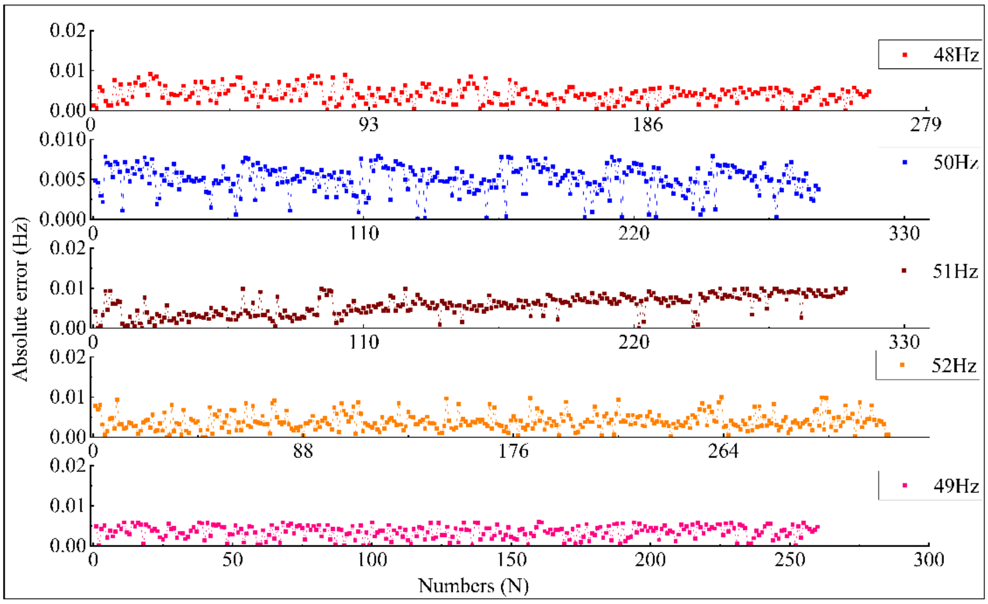

Figure 4.3 The test result of frequency

As shown in Figure 4.3, this study quantitatively analyzes the stability of target frequencies (48Hz, 49Hz, 50Hz, 51Hz, 52Hz) through an experimental system. Each subplot corresponds to measurement results under specific frequency conditions, with the horizontal axis labeled as sample sequence indices and the vertical axis representing the frequency deviation values (Δf) between μPMU and the high-precision digital multimeter. Experimental data indicate characteristic oscillatory patterns across all frequency points. Specifically, under the 48 Hz condition, the deviation values exhibit a fluctuation range of ±0.005 Hz, while the 50 Hz fundamental frequency demonstrates similar amplitude characteristics. Notably, the observed fluctuations at all frequency points display non-uniform distribution properties, which may arise from combined factors such as electromagnetic interference in the test environment and instrumental quantization noise.

Table 4.1 Statistical results of frequency tests

Frequency	Mean	Min	Max
48Hz	0.00411	0.0000746	0.00918
49Hz	0.00355	0.0000553	0.00592
50Hz	0.00453	0.0000136	0.00795
51Hz	0.00391	0.0000255	0.00985

52Hz	0.00491	0.0000485	0.00996

Table 4.1 shows the statistical results of frequency tests, and the results indicate that all the average errors of frequency are less than 0.005 Hz.

B. Amplitude Test

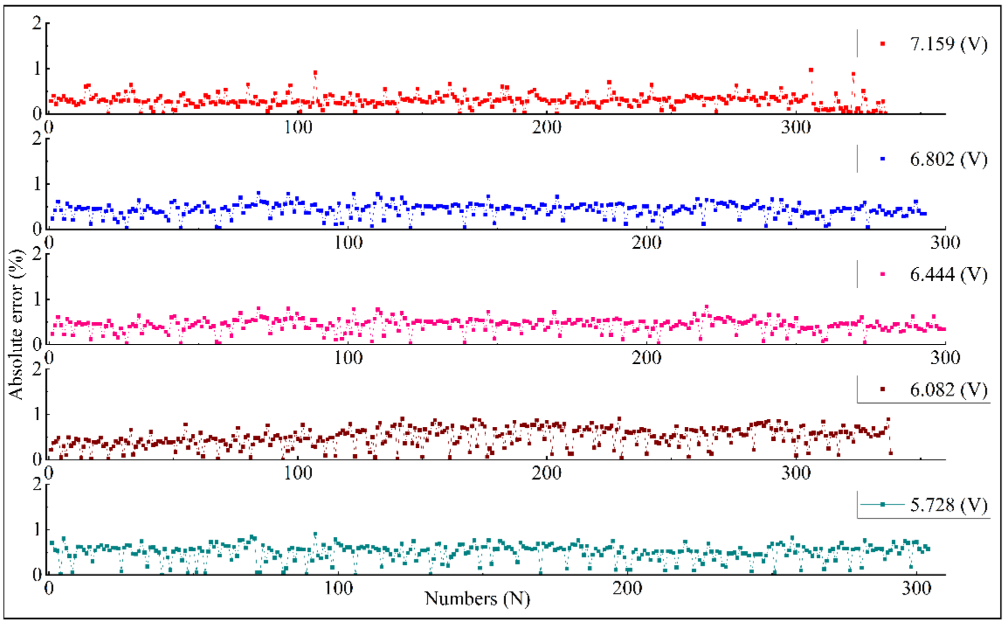

Figure 4.4 The test result of amplitude

As shown in Figure 4.4, this study illustrates the variation of error percentage with sample sequences under different voltage amplitudes, including 7.159 V, 6.802 V, 6.444 V, 6.082 V, and 5.728 V. The horizontal axis represents the sample sequence, and the vertical axis denotes the error percentage. Notably, in all cases, the error percentage remains below 1%, demonstrating a high level of accuracy in the measurements.

Table 4.2 Statistical results of amplitude tests

Amplitude (V)	Mean error (%)
7.159	0.29557
6.802	0.43228
6.444	0.43216
6.086	0.50018
5.728	0.50084

Table 4.2 shows the statistical results of amplitude tests, and the results indicate

that the error centers around 0.5%.

C. Phase test

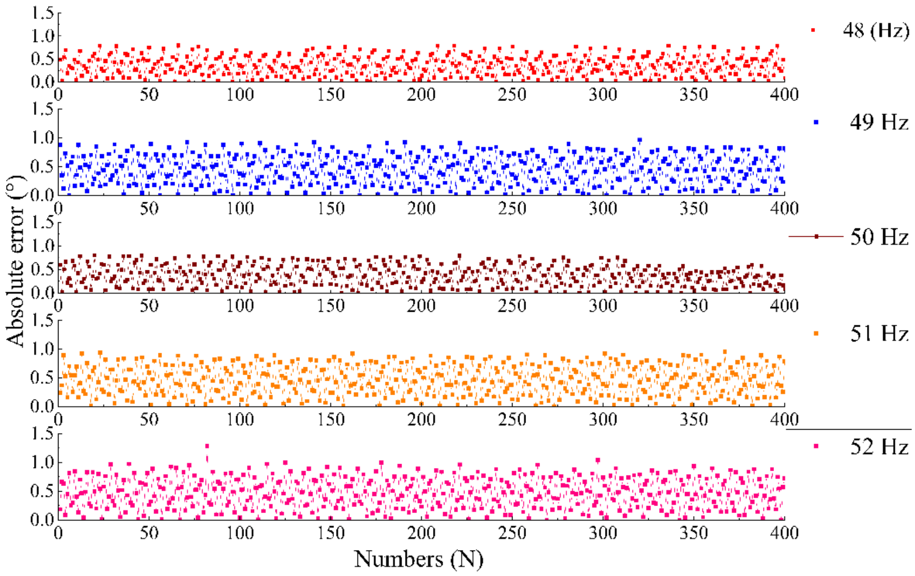

Figure 4.5 The test result of phase

During the phase measurement test, the Pulse Per Second (PPS) signal was connected to the signal generator to synchronize the signal generation timing of the generator with the sampling instant of the PMU. The phase of the signal was set to 90°, and phase angles were measured at frequencies ranging from 48 Hz to 52 Hz. Due to inherent signal delays and phase shifts caused by capacitances in the signal conditioning circuit, a fixed phase offset was introduced. This offset was calibrated to compensate for the systematic error. The calibrated phase angles are presented in Figure 4.5. The measurement phase errors are all less than 1°.

The data statistics of Figure 4.5 are shown in the following table, which indicates that the measured mean values are all less than 0.57°

Table 4.3 The test results of phase degree

Frequency	Mean	Min	Max
48Hz	0.36021	0.00916	0.79751
49Hz	0.44635	0.00271	0.96521
50Hz	0.37343	0.00529	0.79749
51Hz	0.46206	0.00222	0.95436

52Hz	0.47116	0.00103	1.28952

During the Total Vector Error (TVE) testing of voltage signals, time-series data of voltage amplitude and phase were first acquired using a synchronized data acquisition system. Based on the TVE calculation formula specified in IEEE C37.118 standard (Equation 2.3), a computational model was developed using MATLAB 2021b for data processing

$$\mathrm{TVE} = \sqrt{\left(\frac{\Delta V}{V}\right)^2 + \left(\frac{\Delta \phi}{\phi}\right)^2} \times 100\% \tag{3.2}$$

Figure 4.6 shows the normalized TVE test results, where the horizontal axis represents the synchronized sampling time series and the vertical axis denotes the TVE percentage values.

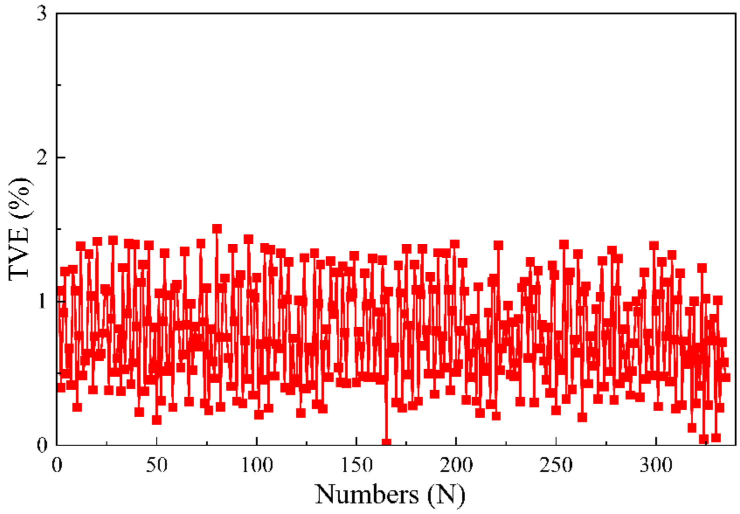

Figure 4.6 The test result of TVE

As shown in the test data of Table 4.4, the system achieved a mean Total Vector Error (TVE) of 0.77975% with a maximum value of 1.503%. By appropriately reducing the TVE accuracy requirement and report update rate, a reduction in hardware cost was successfully achieved.

Table 4.4 Statistical results of TVE tests

	Mean	Min	Max
TVE	0.77975%	0.01145%	1.50351%

In this experimental investigation, μPMU was utilized to conduct dynamic signal acquisition on a 230 V/50 Hz simulated power system within a controlled laboratory environment. Continuous operational data were recorded over a 6-minute interval. The experimental setup is depicted in Figure 4.7.

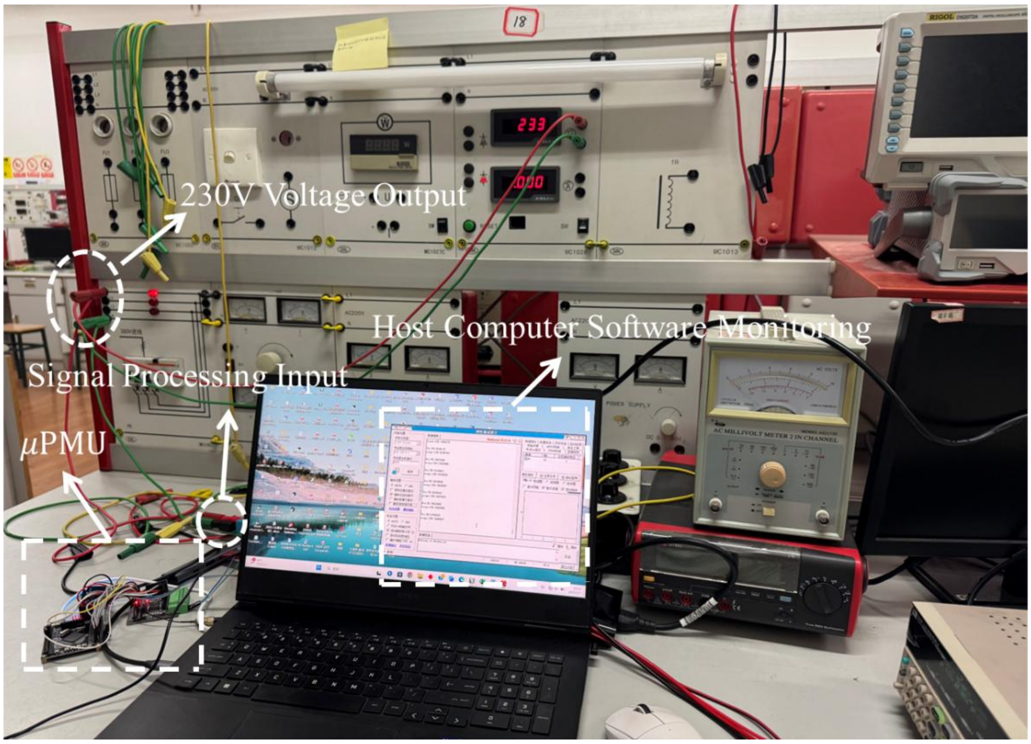

Figure 4.7 The platform of test municipal power supply

A 230 V voltage output was connected to the signal input port of the μPMU, and host computer software was employed to monitor variations in both the amplitude and frequency of the electrical signals. The measurement results are presented in Figure 4.8. The measured data reveal that the steady-state voltage amplitude exhibits a fluctuation rate of $\leqslant$0.2% (229.8–230.3 V), while the steady-state frequency variation remains within 49.9-50.1 Hz. These outcomes substantiate the device’s comprehensive monitoring capability for both steady-state characteristics and transient events in power grid systems, highlighting its precision in capturing multi-dimensional operational dynamics under controlled conditions.

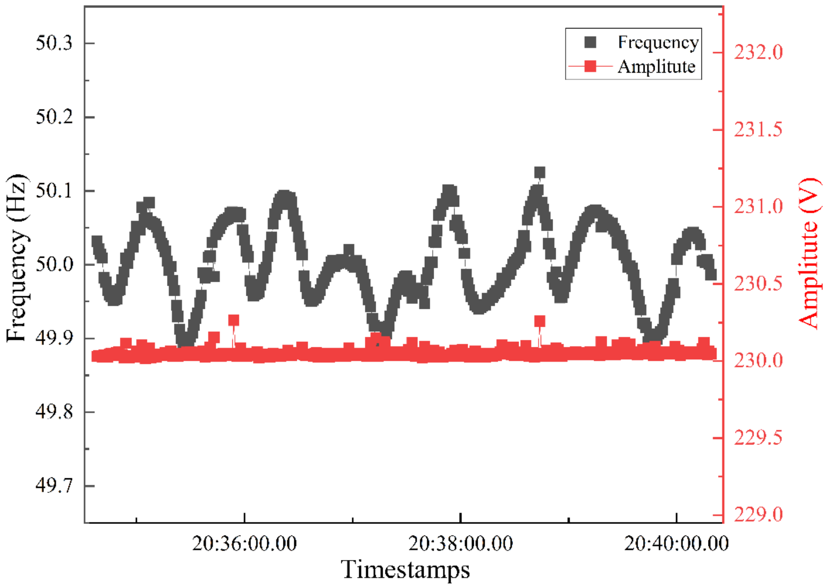

Figure 4.8 Measurement results of the municipal power supply

4.2.2 The test of current

Due to the limitations of available laboratory resources, a voltage-controlled constant current source (KW-BPVCCS1000) is employed as the AC current signal generating device, with its output range limited to ±1 A. This constant current source features voltage control characteristics, where the amplitude of the current output exhibits a linear relationship with the input voltage signal. Therefore, a signal generator is selected as the input device for providing voltage signals to the voltage-controlled constant current source, enabling the output of controllable current signals.

However, practical applications have revealed that the current signals generated by this method suffer from insufficient stability. To ensure the accuracy of test data, it is necessary to calibrate the current signals output by the voltage-controlled constant current source using a digital multimeter. The specific calibration diagram is shown in the following Figure 4.9.

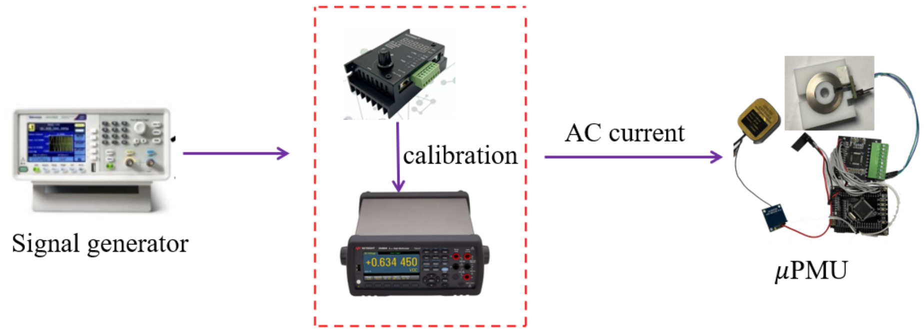

Figure 4.9 The test diagram of current measurement

Based on the technical specifications of the KW-BPVCCS1000 voltage-controlled constant current source (5 V input corresponding to 1 A output), this calibration protocol refines input voltage calibration points with a 0.25 V step increment. Accounting for potential inaccuracies in the manufacturer's documentation, the system establishes 20 equally spaced calibration points across an extended 0-7 V full-scale range. A high-precision digital multimeter synchronously measures the actual output current values at each calibration point, constructing the linear voltage-current correspondence curve shown in Figure 4.8 below. This expanded-range calibration methodology systematically identifies deviations from nominal specifications while mapping the operational characteristics beyond documented parameters, providing critical data for dynamic compensation and system linearization.

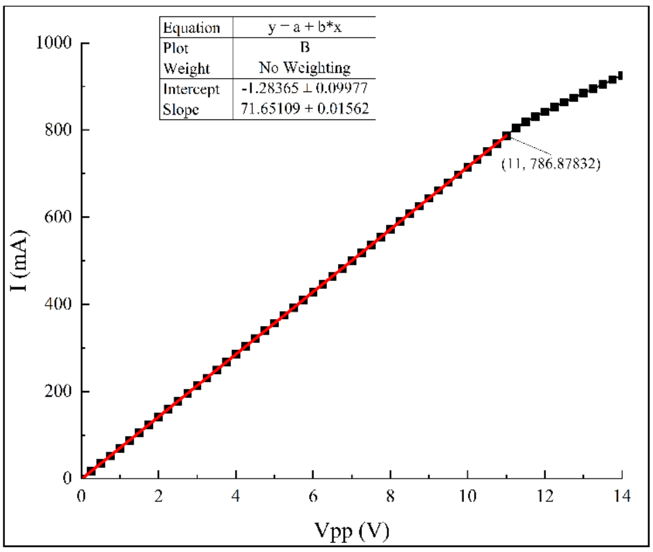

Figure 4.10 The correspondence curve of voltage-current

Experimental data indicate that when the input voltage peak-to-peak (Vpp) reaches 11 V, the system output current measures 786.87 mA. When the input voltage remains below this threshold, the voltage-current characteristic exhibits a highly linear relationship, whereas beyond this threshold, it enters a non-linear region. Based on this characteristic, the system's effective measurement range should be confined to the 0–786 mA interval to ensure operational consistency and measurement reliability.

Amplitude test

The signal generator was configured to output a 10(peak-to-peak) sinusoidal signal. According to Figure 4.10, the corresponding root mean square (RMS) current value is 716.51 mA. Based on the calibration results shown in Figure 3.13, the sensitivity parameter is determined to be 5.2963 mV/V/mT. After calibrating the signal processing board with a digital multimeter, the gain coefficient is determined to be 98.54. The digitized voltage signal acquired by the AD7606 can be reconstructed into current values using Equation (3.2):

$$I = \frac{V_{ADC} - G_{board} * a}{G_{board} * b} \tag{3.2}$$

The V_{ADC} is digitized voltage signal acquired by the AD7606, G_{board} is the gain coefficient of signal processing board, a is the intercept of Figure 3.13, b is the slope of Figure 3.13.

The test results of the current amplitude are shown in the following Figure 4.11

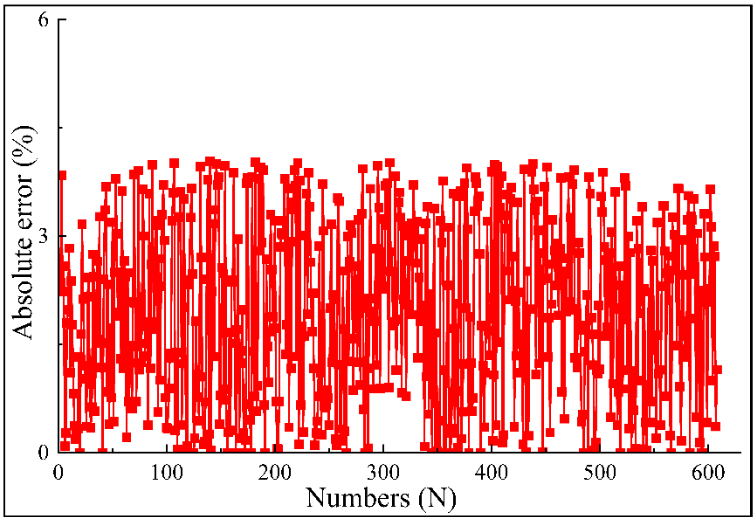

Figure 4.11 The test results of the current amplitude

The mean error in the above Figure is 2.1453%, max error is 4.1542%. Although the current amplitude measurement results of TMR do not meet the measurement standards, there is still considerable room for optimization and improvement in the future. This error may be caused by the insufficient accuracy of the KW - BPVCCS1000 voltage - controlled constant current source and the poor linearity of the TMR.

Frequency test

A comparative frequency measurement of current signals was conducted using a Digital Multimeter and μPMU, with the absolute error between the two methods calculated as shown in Figure 4.9. The experiment employed a multi-frequency comparative testing approach, designing five experimental samples at 48Hz, 49Hz, 50Hz, 51Hz, and 52Hz, each consisting of 360 data points. Under the fundamental frequency condition of 50Hz, the frequency error remained stable at approximately 0.04Hz or less.

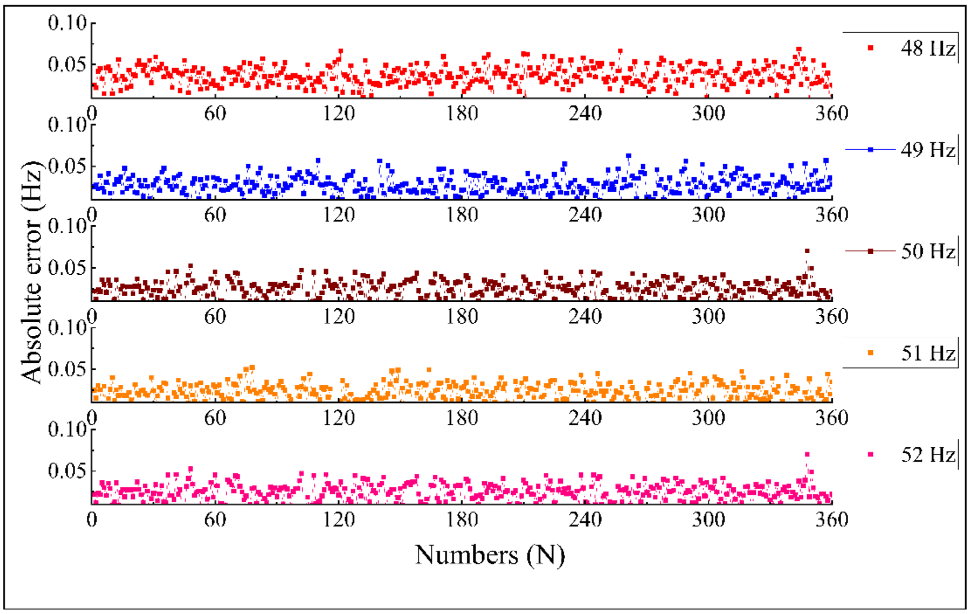

Figure 4.12 The test result of current frequency

Statistical analysis of the data presented in the figure is summarized in Table 4.1. Within the core operational frequency range of 49-52 Hz, the measured frequency fluctuations were consistently maintained below 0.03 Hz. Although the current performance (0.03 Hz) exhibits an order-of-magnitude discrepancy compared to the design requirement (<0.005 Hz), the experimental results demonstrate substantial potential for system enhancement through circuit optimization and measurement architecture refinement.

Table 4.5 Statistical results of current frequency test

Frequency	Mean	Min	Max
48Hz	0.0366	0.0000126	0.06885
49Hz	0.02678	0.0000137	0.06291
50Hz	0.02053	0.0000135	0.04961
51Hz	0.02167	0.0000372	0.05223
52Hz	0.02354	0.0000315	0.07028

4.2.3 Error analysis

The measurement error sources of the micro phasor measurement unit mainly come from the following aspects:

(1) ADC quantization

The primary consideration is the quantization error of the ADC. The analog-to-digital conversion quantization error is a fundamental error determined by the bit resolution of the sampling chip. Due to the finite bit resolution of the sampling chip, rounding or truncation occurs when determining the least significant bit during quantization, inevitably introducing quantization errors. Choosing higher-precision ADCs can mitigate such errors, but higher-precision ADCs also imply increased costs. The 16-bit resolution of the AD7606 contributes a 0.12% TVE, which is a reasonable compromise, as it saves 20% in cost compared to an 18-bit ADC.

(2) GPS timestamp jitter

The timing error of the GPS receiver depends on multiple factors. The typical jitter of PPS signal from a normal GPS receiver is round 10~50 ns. The range of GPS timing errors is set from 5 to 50 ns, it will contribute a 0.07%TVE.

(3) Local clock drift

If cost-saving measures exclude phase-locked loop (PLL) circuitry and instead rely on PPS-controlled local clock-based sampling signal generation, clock deviation becomes a critical concern. This is primarily due to crystal oscillator susceptibility to temperature fluctuations and aging effects. A crystal oscillator with a 50 ppm (parts per million) frequency drift will result in a 0.28% Total Vector Error (TVE), highlighting the necessity of stability-aware design compromises in time-sensitive measurement systems.

Table 4.6 Error contributes to the TVE analysis

Error Source	Contribute to TVE	Mitigation Strategy
ADC quantization	0.12%	18-bit ADC upgrade
GPS timestamp jitter	0.07%	PLL synchronization
Local clock drift	0.28%	Dynamically adjust the frequency or PLL synchronization
TMR sensor	2.36%	Optimize structure

This research focuses on a cost-effective implementation of μPMU. By leveraging commercial off-the-shelf (COTS) components, the hardware cost of this design is controlled within $100. As shown in the following Table, the hardware implementation costs of μPMUs reported in existing literature generally range from $300 to $500.

Table 4.7 Compare of low-cost schemes

Study	Cost	TVE	Reporting Rate	Platform
References [9-12]	$300-500	0.2-0.5%	10Hz	FPGA/DSP/ Raspberry PI
This work	$100	0.78%	1Hz	STM32

Although this work reduced the cost by 60-80% compared with others. The lower reporting rate reflects the computational limitations of STM32. This is a reasonable compromise for distribution networks that require an update frequency of less than 5 Hz.

5. Conclusions

In this study, a low – cost μPMU has been successfully developed. By integrating commercial off - the - shelf components (COTS) and optimizing algorithms, a measurement accuracy with a TVE of 0.78% is achieved, and the total hardware cost is controlled within 100 US dollars, which reduces the cost by 60 - 80% compared with the same type of μPMUs. Through the adoption of TMR sensing technology, the system realizes non - intrusive current measurement. However, limited by experimental resources, it is unable to measure larger alternating currents. In addition, the interpolated discrete Fourier transform based on the STM32F407 microcontroller ensures accuracy while saving more hardware resources and promotes phasor estimation in edge computing.

Table 5.1 Achievement about this work

Objective	Achievement
Develop \$150 μPMU	\$100 prototype
Achieve<1%TVE	0.78%TVE

The current design limitations mainly focus on the absence of current phase angle measurement, which is due to insufficient hardware synchronization calibration under experimental conditions. Meanwhile, the measurement frequency and amplitude results of TMR are not accurate enough, and temperature stability testing has not been carried out. In the future, priority will be given to upgrading the signal conditioning circuit and changing the structure of the current measurement circuit. At the same time, plans are in place to deploy a 10-node μPMU network in the campus microgrid to verify the data synchronization and fusion performance under multi-device collaboration. These improvements will drive the transformation of μPMU from a laboratory prototype to industrial-grade applications.

Against the backdrop of digital upgrading in smart grids, the large-scale deployment of μPMUs offers an innovative pathway for the precise monitoring and reliability enhancement of distribution networks. By widely deploying μPMU, utility companies can replicate the successful experience of PMU adoption in the Italian power grid, achieving a 40% reduction in power outage frequency. The design prototype holds absolute advantages in application scenarios with low PMU reporting rate requirements. For instance, in solar-rich distribution networks that require monitoring of frequency fluctuations caused by granular irradiance, a reporting rate of 1Hz is adequate to meet the needs.

This work bridges the gap between academic micro-PMU research and field-ready solutions, providing utility companies with an affordable template for grid modernization. By prioritizing modularity and commercial off-the-shelf (COTS) components, it lays the foundation for scalable smart grid monitoring in emerging economies.

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